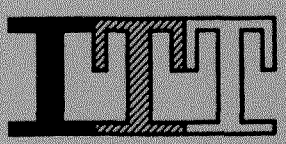
ELECTRICAL COMMUNICATION



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This Issue in Brief

Thin-Film Circuits—A Review—Thin films are layers of conductors and insulators about 1 micron thick deposited on flat surfaces by vacuum, furnace, gas reaction, and plating techniques, with possible modification by etching and engraving, to produce passive integrated electronic structures. The supporting surface or substrate may house diffused semiconductor junctions serving as active elements or such elements made on separate chips may be fastened to the substrate to provide semiconductor integrated circuits. Small size, reliability, and low cost are attained.

Packing densities are about 300 components per cubic inch (18 per cubic centimeter) but may be reduced to accommodate inductance devices like transformers, permit hermetic sealing, and provide increased support for leads. Models for new circuits may be made within a day at low cost, with mass production following immediately. Small components and short leads are ideal for the megahertz range.

Temperature coefficients for resistance and capacitance for those components are typically 50 parts per million per degree Celsius. Parameter drift with temperature and time are small enough to justify adjusting resistors to ± 0.1 percent and capacitors to ± 1 percent of selected values. Capacitors have Q values between 10^4 at 100 kilohertz and 50 at 75 megahertz.

Practical values of inductance are limited to a few microhenries. Q is substantially improved by increasing the film thickness by plating.

Thick-Film Technology—Thick films in microelectronics are obtained by depositing viscous pastes or inks through a fine screen onto a suitable substrate. The material, the pattern in which it is deposited, and the firing temperature that bonds it to the substrate vary with whether a resistor, capacitor, inductor, or connecting lead is desired. The electrical values of components may be adjusted after firing.

Practical values of resistance range from 10 to 10^6 ohms with tolerances of 5 percent as fired and 0.025 percent with trimming. Capacitors using barium titanate as dielectric may range from 100 to 10 000 picofarads and with titanium dioxide from 10 to 1000 picofarads. In both dielectrics, tolerances are 10 to 20 percent as fired and 1 percent with trimming. Spiral patterns are used for inductors but are limited to about 900 nanohenries and are reinforced by solder or plating to improve the Q.

Interconnections for High-Density Packaging—In most applications of integrated circuits, reliability and low cost are of greater importance than small size. The point to which miniaturization can be taken without incurring cost or reliability penalties is largely determined by the interconnection density encountered, and the problem of extracting heat from the equipment.

Examination of the basic topological problems associated with the mounting and interconnection of integrated circuits on printed-circuit cards shows that, although it is theoretically possible to interconnect any number of circuits on a single wiring plane, the solution is impractical. Using two wiring planes interconnected at appropriate points, however, practical solutions are possible, and by providing an orderly matrix of conductors, rationalized interconnection systems result which are very suitable for computer-aided design and manufacture.

The same approach can be applied, in principle, to the pattern required for interconnections between circuit cards.

Improving Performance and Functional Flexibility of Thin-Film and Semiconductor Integrated Circuits—The characteristics of any microelectronic circuit are "frozen in" by the processes used to define the shape of its various layers. This not only places restrictions on the processing of the various layers, but the final function and tolerances of the circuit are determined in the early stages of manufacture. The paper discusses new methods of fabricating both

thin-film and semiconductor integrated circuits which allow greater optimization of the processes and enable the function to be defined towards the end rather than the beginning of the manufacturing sequence.

Thin-film circuits may be fabricated with components whose value, tolerance, and circuit configuration are determined by microengraving after the film deposition processes have been completed. The microengraving process is described in detail.

The application of the concepts to semiconductor integrated circuits is approached by using a cellular universal substrate with a novel isolation technique.

The implications of these new techniques on the manufacture of thin-film and semiconductor integrated circuits are discussed. They affect the redistribution of added value, inventory, and production volume considerations, as well as the time cycle from design to completed devices. Examples of devices whose function is determined by tape-controlled processes are given. This facilitates a transition from design automation to functional system, without the intermediate stages of circuit and component layout drawings.

Flip-Chip Semiconductor Devices—A flip-chip device is a piece of semiconductor material, normally silicon, containing one or more electronic circuit components and having contact pads on one chip face instead of attached leads. These circular contact pads are much larger than the corresponding emitter and base regions of the transistor. This plus the large separations of the 3 contact pads greatly facilitates the attachment of the chip to a circuit.

Typical substrates used are printed-circuit board, metallized ceramic, and metallized glass. The chip has triangles on its back for orientation to the substrate interconnection pattern. Multichip circuits have all active and passive components in chip form.

Typical characteristics of available devices are given, and recent advances in flip-chip technology and directions of potential development are discussed.

Silicon Integrated Circuits—Fundamental circuits are shown for various forms of logic: diode, diode-transistor, direct-coupled transistor, resistor-transistor, resistor-capacitor-transistor, current-mode, and transistor-transistor. Their major characteristics are given.

Operational amplifiers are a significant part of the production of integrated circuits, and means of providing frequency selectivity vary from add-on elements to the use of resistance-capacitance networks that can be provided on the substrate.

Integrated-circuit processing differs from planar-transistor processing only in the method of isolating components. Some of these techniques are described. Packaging has followed transistor requirements, and considerable improvements are possible by adapting integrated-circuit techniques to this problem.

Sandwich-Type Structure Providing Novel Resistor Configurations—With the advent of more-compact microcircuits composed of thin-film components deposited directly on wafers containing isolated semiconductor devices, smaller discrete components become essential. The need for small-component techniques is increased by the development of microwatt circuits which use relatively high-value resistance networks. The use of meandered planar resistors is precluded when the surface area available for the circuit deposition is reduced to that area represented by the top face of a few transistors. High-value resistor networks can occupy 0.5 square inch of surface area, a fact which does not lend itself to integrated microwatt circuit fabrication. This paper presents a possible answer to this problem.

The use of high-value resistors in hybrid integrated circuits is limited by the available surface

area on which to deposit a long meandered thin-film resistor. This limitation can be reversed by constructing the resistors of high-resistivity materials sandwiched between conductors. Whereas planar resistors using the ohm-per-square mode of fabrication require areas proportional to their ohmic value (for a given width), sandwich resistor structures using a mho-per-square-micron mode of fabrication require areas inversely proportional to their value.

Since the value of the sandwich resistor cannot be measured until the second electrode is applied, the resistance value cannot be measured directly during deposition. However, by measuring the resistivity (ohm per square) of a sample resistor and simultaneously measuring the thickness of the deposited film, the resistance value can be instantly calculated by an analog computer circuit.

Selecting Digital Integrated Semiconductor Circuits—The cost of developing semiconductor integrated circuits is so high that standard commercially available units must be employed as extensively as possible.

In an example of a data processing system, the extensive use of gate circuits dictated the selection of diffusion techniques that produce good diodes and transistors at relatively low cost. High immunity to noise generated by electromechanical components in the data system was provided by transistor-transistor and diode-transistor logic circuits. Switching time was satisfactory for both types, and the choice of diode-transistor circuits was made on the basis of better yield in production and a smaller area of silicon wafer per circuit. Heat dissipation was not a limiting factor in this case. Cost determined the use of dual in-line packaging.

Noise Considerations in Microelectronic Digital Computers—The *ITT 9100* store-and-forward computer uses microelectronic digital circuits for economy and reliability. For it, noise is defined as all departures of waveform from the ideal.

A major source of noise is reflections from the ends of unterminated lines. It is directly related to switching speed and voltage and is thus a function of the pulse waveform.

Another major cause of noise is reactance coupling between logic circuits. The capacitance across a minimum etched space between two conducting paths can be of the order of 1 picofarad per inch. Under operating conditions, 1.5 volts can be coupled into an adjacent circuit.

Common ground impedance is the third major source of noise. It is due chiefly to inductance, and resistance plays only a very small part.

It should be noted that noise may reinforce or oppose a desired signal, the latter being the only damaging condition. A figure of merit for noise is discussed.

Microelectronics Applied to an Airborne Photo Data Recorder—Information on date, time, latitude, longitude, altitude, speed, true heading, roll angle, pitch angle, mission number, and identification of the sensor from which these analog signals are obtained is automatically recorded on each photographic negative exposed in an aerial camera in flight. A cathode-ray tube records these data on the film negative in light dots consisting of an indexing dot, 4 dots in excess-3 binary notation, and an odd-parity dot.

The initial design using vacuum tubes was completed over a decade ago. A later all-transistor version weighs 112 pounds (51 kilograms), occupies 3950 cubic inches (65 000 cubic centimeters), and requires 234 watts. The microelectronic equivalent reduced volume to about 400 cubic inches (6500 cubic centimeters), weight to 15 pounds (6.8 kilograms), and replaced several separate units with a single unit. Power consumption was reduced although this was not a critical factor.

Microelectronics Microwave Communication Equipment—Thick-film microelectronics techniques have produced a portable communication terminal providing 300 frequency-division telephone channels or a television channel and an order wire in the 7–8.5-megahertz range. Including self-contained batteries for 5 hours of operation between charges, and a built-in antenna of 26 decibels gain over a dipole, the complete terminal measures 13 inches (33 centimeters) square by 7 inches (18 centimeters) thick and weighs 17 pounds (7.7 kilograms).

Circuit design has minimized the number of components, such as transistors, diodes, inductors, and adjustable units, that must be mounted separately on the microelectronics substrates. The design was based on existing state of the art and not only reduced size and weight but also the cost for large-quantity production.

Integrated Circuits Applied to Pulse-Code Modulation—A pulse-code-modulation system for tactical military operation provides for 12 telephone channels and is extendible to 24 channels. In anticipation of reduced costs of microelectronic elements by the time the equipment would be manufactured, it was designed for use of either conventional components or microelectronic elements as later costs would dictate.

As the half-shift register was the only micrologic element that was already of lower total cost than the corresponding unit using conventional components, maximum use was made of it.

Examples of design include the derivation from a 4.6-megahertz crystal oscillator of all the timing waves and the use of an amplifier that can be switched in gain by coding for level compression and expansion.

Busignies Elected to National Academy of Engineering

Henri G. Busignies was elected a member of the National Academy of Engineering (United States) for his work in aerial navigation systems. He holds more than 140 patents in the fields of navigation, radar, and communications.

He was born in Sceaux, France, in 1905. He received a degree in electrical engineering in Paris in 1926 and joined the Paris laboratories of International Telephone and Telegraph Corporation in 1928. In 1941 he was transferred to the United States to help establish a laboratory for defense. He is now a senior vice-president and general technical director of the parent corporation.

He received the Pioneer Award of the Aeronautical and Navigational Group of the Institute of Radio Engineers in 1959 for his invention of the first automatic direction finder for aircraft and for directing large research and development programs. Among these programs was Tacan, the air navigation system now standard for all United States military aircraft and important elements of which are used by commercial aircraft under the title Vortac.

His contributions to the second world war included moving-target radar and the automatic instantaneous direction finder known as "huff-duff," which proved a vital factor in the war on enemy submarines. For these he received the United States Navy Certificate of Commendation. He also received the Presidential Certificate of Merit for his activities with the National Defense Research Council.

He was awarded an honorary Doctor of Sciences in 1958 by Newark College of Engineering. In 1964 he received the David Sarnoff Award of the Institute of Electrical and Electronics Engineers for outstanding achievements in electronics.

Thin-Film Circuits—A Review

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D. W. GILES
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1. Introduction

Film circuit technology may be said to include all circuit and component forms in which deposited layers of conductors and insulators are patterned to define value and function. Layers deposited by vacuum, furnace, gas reaction, and plating techniques are usually of the order of 1 micron or less in thickness, and are generally termed "thin films." Screen-printed or painted layers are normally described as "thick films" and have layer thickness around 25 microns.

Films deposited on flat plates are used for passive, active, storage, memory, and other devices in a rapidly widening spectrum of integrated electronic structures. Two basic structures have emerged to date.

(A) Film groupings on an inert flat plate substrate which gives mechanical support and electrical isolation or coupling. Examples are passive component networks (resistors, capacitors, inductors), active networks containing thin-film diodes and triodes, magnetic memory arrays, and cryogenic switching arrays.

(B) Film groupings on an active, usually monocrystalline, flat substrate, which houses diffused semiconductor junctions such as semiconductor integrated circuits (*SCIC*).

This artificial division is historical rather than fundamental and may shortly be obscured by a flood of technique permutations.

One requirement for both forms is the ability to deposit and to diffuse layers having controlled shape, thickness, and physical properties. An example of the increasing overlap of technologies is the deposition of nichrome resistors on to silicon chips. Further, the flip-chip transistor mounted on film circuits is almost equivalent to the multichip semiconductor-integrated-circuit approach. For forward planning, they may be considered as facets of one technology—that of making integrated electronic functions. Short term, it is accepted that development effort has been directed into narrow channels for economic and, to some extent, technical reasons.

The motivations for the generation of the overall technology have been successively: miniaturization, reliability, and cost.

Although present trends are mainly influenced by cost considerations, the final situation will be a compromise between all three requirements, and this may be different for each individual application.

One approach to microminiaturization has embodied thin-film circuits, and it is proposed to discuss the origins, merits, and future of this philosophy in some detail. In this system, flat glass or ceramic plates are coated with patterns of high, low, and ultra-low conductivity films whose shapes and areas correspond to the passive component value and power dissipation. Semiconductor and other devices may be added by soldering or welding to complete a functional module.

2. Applications

2.1 General

Over the past 5 years, thin-film circuits have provided miniaturization in prototype military and professional equipment. The deposition patterns have mainly been to the circuit design of customers, who retain the copyright. Standard circuit modules have usually been for evaluation and proof of capability. It is not possible therefore to publish details of the many applications, but the generic types have been in airborne radar (fast logic, also analogue circuits); airborne communications (analogue circuits, strip-line forms); miniature computers (mainly transistor-resistor logic for peripheral equipment and power output situations); and in very-high-speed computers with clock rates greater than 50 megahertz where semiconductor integrated circuits are not suitable.

Apart from component size and quality, the main advantage of thin-film integrated circuits compared with semiconductor integrated circuits has been their potential for providing models rapidly and for economic production of small lots.

Due to early attempts to translate unsuitably designed circuits, there have been unnecessary disappointments. A purist approach has sometimes led to conversion of entire equipments to thin film where partial conversion or combination with other integrated circuits would have been more suitable.

Some examples of thin-film devices are given in Figures 1 through 4.

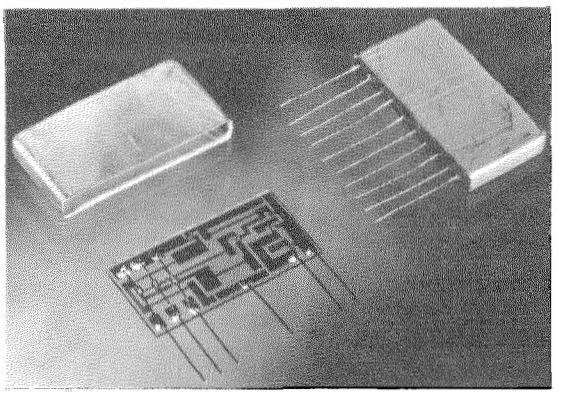

Figure 2—An assembled and an encapsulated switch, with 5 flip-chip transistors and 3 diodes. The encapsulation is silica-loaded epoxy in a deep-drawn can.

2. Distributed-Parameter Devices

Thin-film circuits are likely to be competitive where deposition yields are good and high packing density is achieved. A very favourable application is the distributed-parameter device. One multiterminal film component replaces several discrete components.

Resistor films with 3 or 4 terminals have been designed using our Zebra computer to give π attenuation pads, for example, of 0·5, 1, 2,

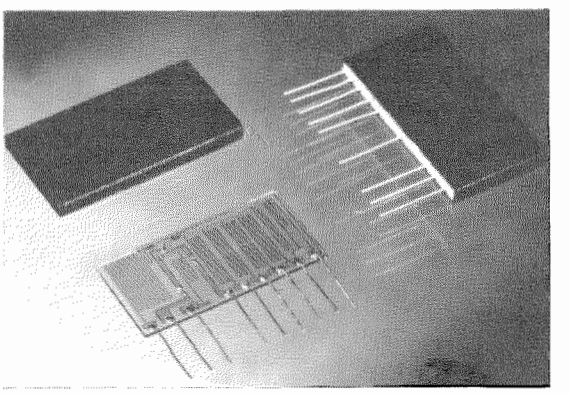

Figure 3—A 5-input logic gate with photo-etched nichrome resistors. A flip-chip transistor can be seen in position.

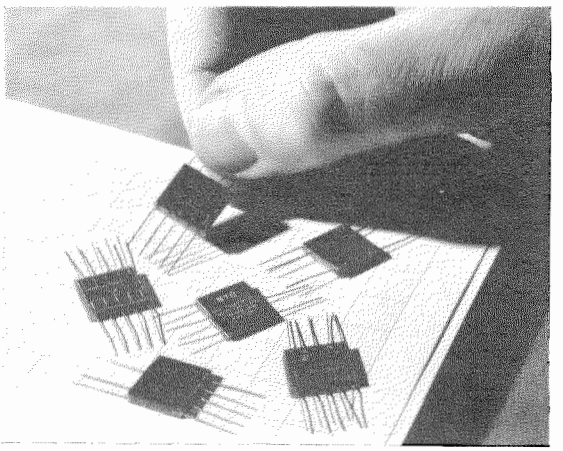

Figure 1—Standard circuit types available from stock. The packing density of resistors, capacitors, transistors, and diodes is typically 300 components per cubic inch.

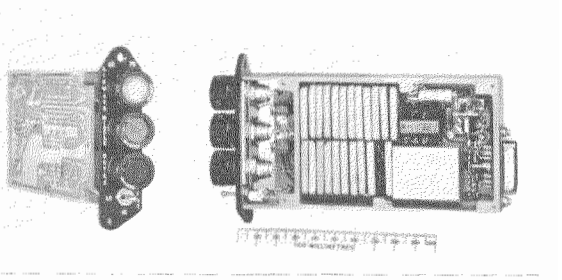

Figure 4—Airborne marker receiver for instrument-panel mounting. There are 16 thin-film circuit packages, the first 5 of which have a gain of 100 decibels at 75 megahertz.

4, 8, and 16 decibels on one plate. Measurements have confirmed the insertion loss and are now directed to the effects of loading and reflected loss.

Thin-film notch filters may be used as alternatives to twin-T networks. Selective amplifiers can be produced, with the filter in the negative feedback loop, as an alternative to inductance-capacitance-tuned amplifiers. For these components, insulating and conducting layers are superimposed such that the resistance layer becomes one of the plates of a film capacitor and a 3-terminal device results. V_{out}/V_{in} reaches a minimum value at the frequency f given by:—

$$f = K/\rho c l^2$$

where K is a constant which depends on the taper of the resistance film, and

ρ = sheet resistivity
c = capacitance per unit area
l = device length.

Similar structures can be used for high- or low-pass filters of phase-change networks. Their feasibility has been demonstrated and their widespread use in professional communication equipment is predicted. Their close tolerances, low temperature coefficients, and low drift rates with time should make them economic devices in the range from 500 kilohertz to 1000 megahertz.

3. Attributes of Thin-Film Techniques

3.1 Cost

In relatively few applications, film circuits may be preferred for their small size and reliability alone. It has become increasingly obvious, however, that major usage arises from the ability to compete on cost with alternative integrated- and discrete-component constructions. Because most depositions in vacuum are batch processes, the number of circuits per batch has a direct bearing on cost. This can be broken down into the area per circuit and the area of uniform deposition in a system. These factors have stimulated increased utilization of substrate area, for example by the use of microphotography and chemical etching and now by microengraving. The component size must not be reduced below the point at which yields fall off due to loss of dimensional control, and also below which long-term stability and reliability may be affected by substrate imperfections and edge effects.

Where cost is of paramount importance, some active and other components will be mounted external to the film-circuit module because of their high relative cost and the effect on yield at final assembly.

3.2 Reliability

The packing densities that initially achieved 300 components per cubic inch (18 per cubic centimetre) have been marginally decreased in some cases: firstly to extend the capability by the inclusion of an added component, such as a radio-frequency transformer; secondly for increased reliability through hermetic sealing or to provide additional support for lead wires.

The monolithic structure and the small number of materials and material boundaries are cogent reasons for the inherent reliability of thin-film passive networks. The substrate is chosen for its strength, thermal properties, weatherability, resistance to chemical attack, and low free-ion content.

For deposited materials, we have typically nickel-chromium (used for years for high-stability wire-wound resistors), and alternatively the valve metals such as tantalum, noted for stability. The use of noble metals (gold or platinum) for conductors eliminates electrolytic attack and can be economic due to the small quantities used. Quartz and tantala have heats of formation of $2{\cdot}1 \times 10^5$ and $4{\cdot}92 \times 10^5$ calories per gramme-mole respectively, giving long-term stability and closely predictable properties for dielectrics. Thermal expansion mismatches have decreased significance in thin-film structures.

Since the materials are fractionally distilled in vacuum, close manufacturing control is possible and this is another highly significant factor in the attainment of reliability. The original basic aim has been to develop components which are stable and reliable with no encapsulation, and then to encapsulate them in an impervious system. The degree of achievement of this aim is limited by economic factors, but parity (or better) with high-quality discrete components has generally been maintained.

Economic considerations restrict the extent and delivery needs restrict the duration of the reliability testing of circuits manufactured in small quantities. Designs in this category can be examined by the following system:

(A) Use of known and proved discrete components.

(B) A thermal plot of working circuits to locate any hot spots introduced by a particular design.

(C) Rapid temperature cycling (for example, in a silicone oil) of working circuits to locate unreliable structures due to thermal expansion mismatches.

(D) Step stress tests.

Having proved a design, close quality control of production circuits is necessary to minimize circuit failures in the field. For any component, there are generally three phases in life. The initial period in which a relatively high number of failures occur due to errors in manufacturing; the main phase, which has generally shown very-low failure rate; and the final or end-of-life phase, which commences when the failure rate increases due to wear-out.

Our experiments with thousands of thin-film components using quartz-dielectric capacitors and nichrome resistors have not detected wear-out mechanisms in periods of up to 26 000 hours for unprotected devices. The drift rates of the parameters have been shown to be very low and in fact tend to stabilize with time.

Minimum handling and no measurements are made before the thin films are mechanically protected by evaporated layers of silicon monoxide. A 100-per-cent visual inspection with magnification ensures that outlines and designs are preserved. Functional tests and destructive tests on samples after each of the few manufacturing processes are not prohibitively expensive in this system. The encapsulated circuit modules are then given the normal temperature cycling and physical examination before the final electrical test.

The individual measurement and the precise performance of thin-film components make the prediction of circuit performance compatible with the systems used for discrete components.

With time, the variations in circuit performance over the full temperature and frequency ranges that are introduced by semiconductor devices far outweigh those of the passive-film components.

3.3 Miniaturization

Thin-film circuits are designed for minimum substrate area compatible with power dissipation, for tolerances governed by geometric accuracies, and for minimum track width limited by defects on the substrate surface.

In setting these minima, it is important to differentiate between what is technically possible and what can be sold as a reliable article at a competitive price. For economic yield, tolerance, and reliability, a resistor track width is not normally less than 4 mils on a glass substrate having a finish of about 5×10^{-7} inch and not less than 10 mils on a ceramic substrate with 30×10^{-6} inch finish (Figure 5). Both figures are root-mean-square and refer to short-pitch roughness.

The present state of the art is such that there are now several material systems capable of producing thin-film resistors and capacitors with a greater stability than many conventional components. Comparative data for thin-film components and techniques are given in Tables 1 through 3.

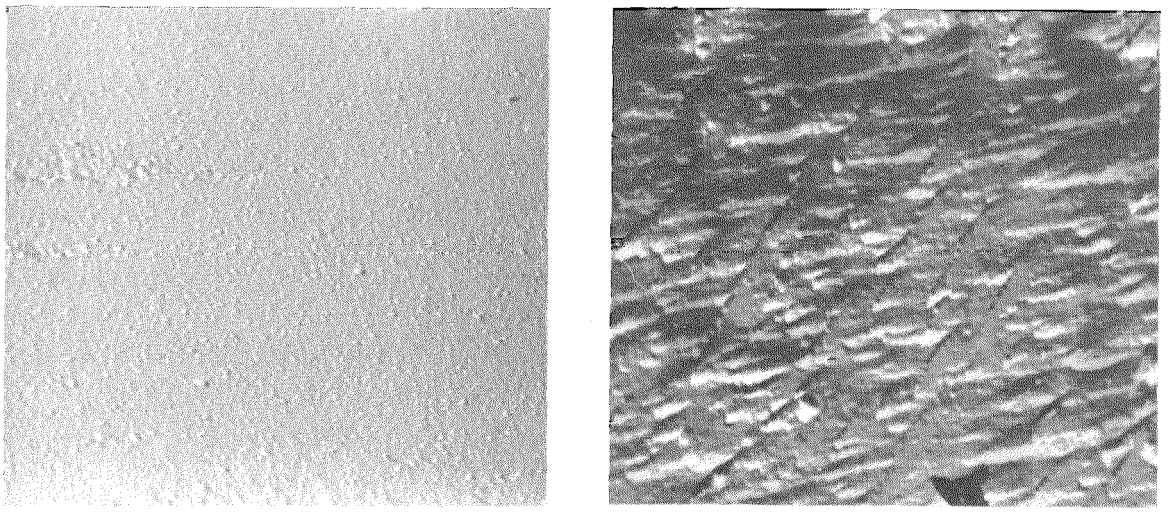

Figure 5—Electron micrographs using carbon replicas of substrate surfaces before deposition. Magnification is 20 000 times in each case. At left is Corning *0211* glass substrate and at right is American Lava glazed ceramic.

TABLE 1

COMPARISON OF RESISTOR PROPERTIES FOR INTEGRATED CIRCUITS

Resistor Material	Thin Films			Thick Films	Semiconductor Circuits	
	NiCr	CrSiO	Ta_xN	PdAg on Glass	Diffused	Evaporated
Sheet resistivity (ohms per square)	300	3000	20	1 to 20 000	100 to 250	50 to 250
Range of values (ohms)	15 to 10^6	160 to 10^6	10 to 10^4	200 to 500 000	100 to 30 000	100 to 100 000
Power dissipation (milliwatts per square centimetre)	300	300	4650	250 each	150 milliwatts total	150 milliwatts total
Temperature coefficient (parts per million per degree Celsius)	+50	−150	+50 to −250	±200	+2000	±50
Maximum temperature coefficient ratio (parts per million per degree Celsius)	20	40	40	—	±300	±10
Tolerance, ex plant (± per cent)	5	10	10	20	20	10
Tolerance, adjusted (± per cent)	0·05	1	0·02	0·25	ratio 10	ratio 10
Noise (microvolts per volt)	0·01	—	0·01	comparable	—	—
Voltage coefficient (per cent)	0·003	—	0·003	0·02	*	*
Drift at rated load in 1000 hours (per cent):						
100 degrees Celsius	<0·1	0·5	0·1	0·5	<1	<1
25 degrees Celsius	<0·1	0·5	0·01	0·5	<1	<1

* There is an associated capacitance proportional to resistor value and determined by the voltage gradient along the resistor.

The gap between adjacent film tracks can be designed down to 2 mils for the low voltages normally used in transistor circuits.

The module thickness is largely determined by the size of the added components and the degree of protection required, being generally 5 times the substrate thickness.

3.4 Flexibility of Design

The inherent flexibility of thin-film circuits permits decentralized fabrication. A breadboarding facility is essential as, unlike semiconductor integrated circuits, thin-film circuits consist of precise components directly interchangeable with conventional components. A new spark machining technique called "microengraving" enables conversion from design to module to be completed within one day or less with low investment cost and a minimum of special skills. The equipment designer is thus able to produce quickly a working circuit from one of a small range of standard thin-film substrates. Both resistors and capacitors can be defined in value and manner of connection. Since both types of component are not sensitive to moisture and are stable in value without encapsulation, a prototype equipment can be assembled with a minimum of facilities and remote from the large-volume capability.

Alternatively, microengraving can be used to obtain photographic masters of a size for sequential photochemical etching—again direct from punched-tape data.

A direct design link from the computer to the actual circuit may therefore be only a short way ahead for thin-film circuits.

3.5 High-Frequency Performance

The miniaturization effect can be used in computers to reduce propagation delay and pulse

Table 2
Comparison of Capacitor Properties for Integrated Circuits

Capacitor Dielectric	Thin Films			Thick Films	Semiconductor Circuits	
	SiO_2	Silicon Monoxide	Ta_2O_5	Barium Titanate and Glass Frit*	p-n Junction	Passivating Oxide Layer
Specific capacitance (picofarads per square millimetre)	50 to 100	50 to 100	620	50/mil	1 to 200 picofarads total	1 to 100 picofarads total
Working volts (volts)	12 to 6	—	15	30	10 polar	10
Dielectric constant	3·8	4 to 4·5	15 (27)	5×10^3	—	4
Tolerance, ex plant (± per cent)	5	10	5	20	20	15
Tolerance, adjusted (± per cent)	0·5	—	—	—	—	—
Q (cot δ):						
100 kilohertz	10^4	10^3	100 to 200	80 to 100	—	—
1 megahertz	10^3	700	30 to 200	—	—	—
30 megahertz	200	—	—	70	—	—
70 megahertz	80 to 100	—	—	1 to 5	—	—
Leakage current for 0·1 microfarad at 10 volts (amperes)	$<10^{-11}$	$<10^{-9}$	$<10^{-9}$	—	10^{-6} to 10^{-10}	—
Typical temperature coefficient (parts per million per degree Celsius)	20	50	250	−200 to +1000	200	—
Voltage dependence	—	—	—	negligible	$C=\frac{K}{(V+V_d)^{-1/3}}$	—

* Tentative data.

energy. This is particularly important in high-speed circuits since the group velocity of an electromagnetic wave travels only about 10 inches in 1 nanosecond. This period of time is of the same order as the switching time of the fastest transistor circuits. The self-capacitance of each lead wire is an energy sink for logic pulses, therefore size reduction has a significant effect on overall system speed.

Low self-capacitance of thin-film resistors and conductors, due to small size and planar configuration, improves the performance of very-high-frequency linear circuits. The area shape factor has a greater influence on the degradation at high frequency than the component value. The parasitic reactance is invariably of capacitance for resistors, being typically less than half a picofarad. The finite resistance of thin-film conductors has to be included in the design consideration for some circuit elements; for example, electrodes for thin-film silica capacitors used in 75-megahertz tuned circuits, and

TABLE 3

CIRCUIT MANUFACTURE BY FILM TECHNIQUES

	Thick Film, Cermets	Tantalum	Nichrome on SiO_2
Substrates	unglazed ceramic	glass, glazed or lapped ceramic, lapped sapphire	glass, glazed ceramic
Substrate preparation	common techniques using ultrasonics and vapour degrease		
Resistor deposition	screen print	in vacuo	in vacuo
stabilization	belt furnace	anodization	static oven
Conductor deposition	screen print	in vacuo	in vacuo
stabilization	belt furnace	—	—
Capacitor deposition:			
lower electrode	screen print	in vacuo	evaporation in vacuo
stabilization	belt furnace	—	—
dielectric	screen print	anodization	sputtering in vacuo
top electrode	screen print	evaporation in vacuo	evaporation in vacuo
stabilization	belt furnace, no burn-out	burn-out (electrical)	burn-out (electrical)
Protective coating:			
deposition	screen print	nil	evaporation in vacuo
stabilization	belt furnace	—	—
Passive component test	common techniques using probes, bridges, et cetera		
Adjustment (for 90-per-cent circuit yield, 6 resistors)	*airbrasive*	*anodizing*	*microengraving*
±20 per cent	not required	not required	not required
±10 per cent	individual	not required	not required
±5 per cent	required	collective	not required
±1 per cent	required	individual	individual
±0·1 per cent	not feasible	individual	individual
Assembly:			
added components	soldering	soldering, welding, or bonding	soldering, welding, or bonding
lead wires	soldering	soldering or welding	soldering, welding, or bonding
Encapsulation:			
entertainment	epoxy dip or rubber cast or epoxy cast		
military and professional	common techniques using epoxy cast or hermetic cans		
Functional tests	common techniques using functional test gear		

emitter connections to transistors in grounded-emitter configurations (Figure 6).

The application of strip-line resistors and interconnections up to and above 1000 megahertz is a growing activity. Increasing frequency demands increasing component accuracy and stability and an absence of strays—advantages that thin films have over thick films, semiconductor integrated circuits, and discrete components.

4. Component Characteristics

4.1 Resistors

All thin resistance films in general usage have temperature coefficients nearer to zero than the bulk parent material. Nichrome films of 300 ohms per square on glass substrates have a value typically 50 parts per million per degree Celsius while the value of the bulk material is 400 parts. The conduction mechanism here is complex, with contributions by metallic conduction and electron tunnelling across gaps in the discontinuous film. The temperature coefficient is also depressed by surface effects since the film thickness is less than the mean free path of the conduction electrons. The worst-case figure for drift of resistance of unprotected nichrome film is 0·1 per cent per thousand hours with an electrical load of 2 watts per square inch (0·3 watt per square centimetre) of resistor area in an ambient temperature of 100 degrees Celsius. This rate falls progressively to an overall value of 0·05 per cent per thousand hours at 20 000 hours. The voltage coefficient is typically 0·003 per cent for these resistors, with noise at less than 0·01 microvolt per volt.

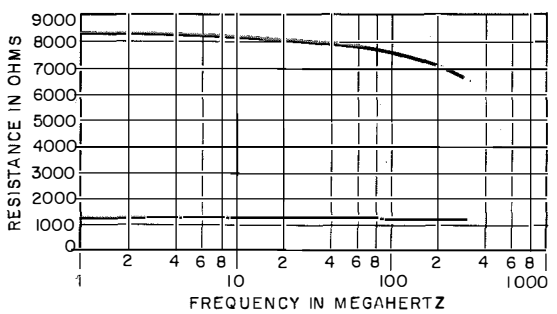

Figure 6—Variation of nichrome resistors with frequency, showing increased change for multi-track higher-value resistor.

The low drift rate of parameters and the low temperature coefficient of film resistors enable them to be practicable down to selection tolerances of 0·1 per cent, which is readily achieved by microengraving for nichrome and anodization for tantalum. The difference in temperature coefficient for two nichrome resistors on the same substrate is at worst 20 parts per million per degree Celsius, and a 50-degree difference in temperature across the substrate would thus produce a 0·1-per-cent change in the ratio during each 5000 hours working.

Much of what has been said also applies to tantalum film resistors between 30 and 100 ohms per square. This metal, like nichrome, has a high resistance to corrosion. It is sputtered in a controlled argon and nitrogen atmosphere over large substrate areas. Pattern outlines are obtained by removing unwanted tantalum in a few seconds by etchants based on hydrofluoric acid. Precise resistor values are obtained by the degree of anodization. This is monitored on one resistor per substrate for 5-per-cent resistors and on each resistor if 0·1-per-cent tolerance is required.

It is worth noting that accuracies and stabilities of the above orders are not yet achieved by thick films on ceramic substrates or by diffusion in silicon planar semiconductor integrated circuits. Thin-film resistor deposition on the oxide used to protect planar semiconductor integrated circuits forms a useful combination, but this technology must accept severe limitations of power and area usage for cost reasons.

The evaporation of a chromium-silicon monoxide cermet also produces reasonably stable resistor elements. A typical result for films of 200 ohms per square gives a stability of 2 per

cent for resistors in the very high ambient temperature of 300 degrees Celsius for 1000 hours. It is interesting to note that there is a second stable region at 3000 ohms per square for this cermet, which coincides in resistivity with the most stable thick-film resistors made by screen-printing palladium-silver and glass frits on alumina substrates and firing them at 750 degrees Celsius. The nature of the conduction mechanism may provide the clue to what, at first sight, appears a genuine coincidence.

4.2 Capacitors

An all-dry process of capacitor manufacture is by reactively sputtering a cathode of silicon in 50 microns pressure of oxygen to make a quartz dielectric layer. Aluminium electrodes are evaporated through stencil masks before and after the quartz deposition. The moisture-resistant layers of quartz (stoichiometric silicon dioxide) are also deposited through stencil masks and have a dielectric constant of 3·8. A typical specific capacitance is 50 picofarads per square millimetre (0·03 microfarad per square inch). Selection tolerances of ±5 per cent are achieved at high yield ex plant with adjustment to ±1 per cent by microengraving. The Q (reciprocal power factor) of the capacitors is typically 10^4 at 100 kilohertz, falling to 50 at 75 megahertz. The capacitance drift rate with time has a worst-case value of −0·06 per cent per 1000 hours up to 20 000 hours at normal 6-volt stress in an ambient temperature of 85 degrees Celsius. There is no observed degradation of power factor with time up to 26 000 hours, which covers the above tests.

The temperature coefficient of capacitance is linear over the operating range and less than 50 parts per million per degree Celsius.

A faster method of depositing the dielectric is by evaporating a mixture of silicon and silica. The resulting dielectric, $a\,\mathrm{Si} + b\,\mathrm{Si_xO_y} + \mathrm{SiO_2}$ is commonly called silicon monoxide. The colour and dielectric constant of this material vary with the oxygen content, which is determined by the degree of dissociation in the source and the recombination at the substrate.

Very close control of source geometry, source temperature, deposition rate, and residual gas atmosphere, for example, has to be maintained for the dielectric constant to be reproducible within 5 per cent.

A wet manufacturing cycle for capacitors is the pattern etching and surface anodization of sputtered tantalum films. The nitrogen-doped films for stable resistors can be used, but the lowest-loss capacitors are produced by anodizing pure tantalum. The effective dielectric constant depends to some extent on the counter-electrode. A value of 15 with aluminium counter-electrodes gives a specific capacitance of $0{\cdot}05/V$ microfarads per square millimetre, where V is the anodizing voltage.

Leakage currents of less than 10^{-9} ampere per microfarad-volt have been achieved with up to 50 per cent of the anodizing volts applied, when the tantalum films were low-pressure sputtered—a new and promising technique.

Reactively sputtered tantala capacitors are non-polar but have lower working voltages than anodized devices of the same film thickness.

Higher specific capacitances have been obtained with titanium compounds but this work is in an early stage of development. The main problem is recombination and stoichiometry of the deposited films. The electrical parameters are critically dependent on crystal structure and oxygen content.

4.3 Inductors

Planar configuration restricts the fabrication of film inductors to a few microhenries—due firstly to cost and miniaturization requirements and secondly to performance.

Stress and cost considerations limit the usable film thickness of conductors ex-vacuum deposition to the point where Q values are typically below 15 at 30 megahertz. Plating-up tech-

niques have been developed which permit Q values over 50 at 100 megahertz.

In general a high Q can be obtained if the film thickness is greater than twice the skin depth at the operating frequency. This is given by

t = constant x (frequency)$^{-1/2}$, in centimetres.

The constant is 7·3 for gold, so that at 50 megahertz the inductor film thickness must be more than 10 microns and at 5 gigahertz more than 1 micron. With this design a Q value over 150 is obtained.

4.4 Active Devices

A wider range of applications for thin-film circuits will be possible when active devices are manufactured in quantity on the same low-cost substrates as passive components.

Packing densities up to a thousand amplifier stages per square inch have been reported for those evaporated polycrystalline thin-film transistors which are in the most advanced development stage. The problems preventing rapid exploitation are all in manufacture, namely:—

(A) The accurate location and reproduction of the 5- to 15-micron gap between source and drain electrodes.

(B) Reproduceability in depositing semiconductor and insulating films, particularly their stoichiometry.

(C) Loss of performance in the presence of moisture.

(D) Consistency of surface structure of low-cost substrate.

New methods of deposition and pattern definition are being developed with the potential of either solving or reducing the influence of these problems.

Other structures nearer to conventional transistors in concept require the deposition of single-crystal semiconductor areas on a low-cost passive substrate. Until a major breakthrough is obtained, this particular approach seems doomed to remain in the laboratory.

The position may be summarized as being developmental with the strong possibility of application below 1 megahertz in 3 to 5 years.

5. Manufacturing Materials and Techniques

Much argument has centred on the relative merits of various substrate possibilities. These are:—

Glass (borosilicate, alumina-borosilicate)
- Lapped
- Flame polished
- Vacuum cast

Unglazed ceramic (alumina, beryllia, barium titanate)
- Rolled and fired
- Lapped

Glazed ceramic (alumina)
- Fired

Quartz
- Lapped

Sapphire
- Lapped

Flame-polished glass has so far provided the best and most economic surface for films below 500 angstrom units in thickness, due to its extreme smoothness and relative freedom from micro-fissures.

Glazed ceramic surfaces have not so far proved satisfactory for very thin films due to differential expansion and hence surface imperfection problems. As surface roughness increases, control of film resistivity and temperature coefficient becomes worse due to changes in the conduction mechanism.

Lapped surfaces, particularly sapphire, can provide satisfactory finishes, but extreme care and considerable expense are required to achieve them. The stability of tantalum resistors has been shown to be better on lapped sapphire than on glass or glazed alumina. Unfortunately, the incidence of rogue failures on sapphire proves significantly higher—probably due to random micro-scratches which are difficult to eliminate entirely from mass-production polishing operations.

Lapping operations applied to glass may expose micro-bubbles which are conveniently covered over by flame polishing—for this and the above reasons, lapping it is not usually recommended.

Ceramics generally permit a 100-per-cent increase in dissipation per unit area of resistor compared with glass, but overall circuit dissipation severely limits the degree to which this advantage can be utilized for space economy.

Sintered ceramics are mechanically more robust than glass and, for film thicknesses above 1000 angstrom units where an unglazed surface finish of 30 micro-inches is usable, are to be preferred. Unfortunately this rules out most thin-film resistor materials and also those required for making stable thin-film capacitors.

5.2 Patterning

Patterning is perhaps the most important single technology apart from deposition, since it is amenable to computer control.

5.2.1 *Stencil Masking*

This method requires accuracies of mask slot width around ±0·0005 inch (±0·013 millimetre), which for minimum slot widths of 0·010 inch (0·254 millimetre) represents 5-per-cent tolerances. Steel, molybdenum, nickel, and copper are all widely used in thicknesses ranging from 0·0002 to 0·0030 inch (0·005 to 0·076 millimetre). Masks are produced by photo-chemical methods appropriate to printed-wiring boards, but under closer control.

If slot widths are kept above 0·015 inch (0·38 millimetre), multiple 5-per-cent resistor groupings can be made with deposition yields over 80 per cent.

5.2.2 *Photo-Etching*

Widely used and flexible in application, photo-etching requires less tooling but extra processing for each circuit, compared with stencil masking.

Early work was confined to a process known as in-contact masking in which a thin metal layer, typically copper, was temporarily deposited and photo-etched to form an in-contact stencil mask. In deposition the desired resident material then adhered to the glass where permitted, while all material arriving on the temporary mask was lifted away by subsequent etchant attack on the latter.

This method proved expensive and has been superseded by a range of selective etching processes. Metals and insulators are deposited sequentially all over a substrate during a vacuum cycle. Photo-chemical resist and etching processes are then used to attack and pattern each layer in turn, without affecting other layers present. The method offers excellent modelling possibilities for equipment manufacturers—using supplies of pre-deposited substrates manufactured under close control by thin-film component makers. Component tolerances of 10 per cent with track widths of 0·005 inch (0·13 millimetre) are practicable.

The ability to process large surface areas at one time makes photo-etching attractive in production.

5.2.3 *Electron Beam Machining*

Methods using either beam deflection or moving work-tables in vacuo have been deployed experimentally. The method appears amenable to computer control of pattern, but for beam deflection, spot size is affected by beam deflection angle which may reduce accuracies theoretically obtainable.

Re-evaporation of materials hit by the beam generates a debris problem, while thermal shock damage to the substrate material presents further difficulties.

A scanning electron beam for exposing photo-resist has also been used experimentally and promises high resolution.

Equipment for this technique may cost between $50 000 and $70 000.

5.2.4 *Ion Beam Deposition*

A method in which material evaporated in a plasma becomes ionized and is directed into a programmable beam of metal has been shown to be feasible. No practical solutions to the main problems are yet in sight, and high on the list is the need to dissipate the large incident energy of material arriving at the substrate. Damage to previously deposited materials is incipient.

The method, if it can be made to work, has the principal advantage that it is additive. Material is deposited only where it is required. Deposition and patterning equipment is again likely to be very costly.

5.2.5 *Microengraving*

A refined form of spark machining is a comparative newcomer. It permits low-cost resolution and miniaturization comparable to photoetching, but avoids chemical processes.

Cutting speeds up to 0·4 inch (1 centimetre) per second in resistor material, and cut track widths of 0·001 inch (0·025 millimetre) upwards with insulation resistance of 10^{11} ohms per inch (4×10^9 ohms per millimetre) are practicable due to oxidation of micro-debris.

Used in conjunction with a stepping motor-operated x-y co-ordinate table, the method has been shown suitable for punched-tape control.

With pre-deposited substrates and master patterns, film circuits can now be made by remote control using telex facilities directly coupled to a microengraving machine located at a distance.

The two main advantages of this system are that the process can be used to make circuits or photo masters direct from punched tape (no drawings are required) and that the process, unlike ion or electron beam methods, can be in air. Compared with the latter, the cost of automatic on-line control equipment is one order less.

5.3 Assembly Techniques

A wide variety of active and passive components have been attached to film circuits but with mixed success. These range from *TO-18* encapsulated transistors and electrolytic capacitors to silicon semiconductor chips.

Most users favour soldering for lead attachment since it caters for almost all lead materials and sizes. Welding provides good joints for connections internal to the module, but it has not proved practicable to weld large lead wires to thin conductor films with sufficient strength to meet external requirements.

Transistor flip-chips can be soldered directly to suitably prepared conductor patterns with efficiencies of mounting in production near 99 per cent per joint. A semiconductor integrated circuit with 14 connections would, on this basis, have a mounting yield of 85 per cent. Similar results are being achieved experimentally by ultrasonically bonding plated-up pillars of aluminium or gold on the substrate or chip to appropriately placed complementary pads.

The inversion and rigid mounting of multiple-lead semiconductor-integrated-circuit chips to film circuit substrates raises severe yield and mechanical expansion problems. It is likely that some form of flexible lead directly linking evaporated pads on chips and film circuits will prove more reliable in this instance.

The price of transistor and diode chips has remained disappointingly high. This is mainly attributed to the increased area of silicon required to make a flip-chip version of a conventionally mounted device and also to the difficulty of testing chips with solder-coated contact areas.

The range of flip-chip devices available has, until quite recently, remained small. There are speed and power limitations which arise respectively from increased pad size (which increases capacitance) and from chip inversion (which limits effective heat transfer from junction areas).

6. Future

At present over 85 per cent of electronic circuits in use are analogue. Despite a decrease in this percentage due to a wider use of digital conversion techniques, the opportunities for application of both thin- and thick-film circuits will expand.

It is of interest to note that, for the whole of 1965, sales of all types of film integrated circuits in the United States exceeded those of all semiconductor integrated circuits by a factor in excess of 3 to 1. Allowing for the fact that the larger part of these sales were for thick-film circuits, it would nevertheless appear that the predictions made in this field will be shown to have under-estimated the impact of film circuits on the integrated-circuit market.

It is also likely that this state of affairs will continue, since the invasion of the digital field by semiconductor integrated circuits will be matched by an increasing use of film circuits in the professional and entertainment fields—again, mainly thick films.

The particular impact of thin-film circuits will be strongest in these applications:—

(A) Where one film circuit component can replace several discrete components and thus compete in cost.

(B) Where miniaturization is more important than cost.

(C) Where the highest stability and accuracy in passive circuits are required.

David Boswell was born in London. After war service in the Royal Air Force with the rank of Flight Lieutenant, he obtained his Bachelor of Science engineering degree at Queen Mary College, University of London, in 1947.

With the General Electric Company Research Laboratories, he worked for 12 years on a wide range of projects, the last 3 years of which concerned semiconductor devices. In 1959 he joined the then newly formed Associated Transistors and in 1961 he started the Microelectronics Research Division of Elliott-Automation, setting up thin-film and semiconductor-integrated-circuit activities.

He joined Standard Telephones and Cables in 1965 and is at present Manager of the Film Circuit Unit at Paignton, Devon, developing production capability for both thin- and thick-film circuits.

He has been active in both national and international standardization in the field of microelectronics and has represented the United Kingdom at such meetings in the United States.

Derek W. Giles was born in Spalding, England, in 1929. The award of the Cooper Scholarship to Nottingham University resulted in an Honours Degree in Physics. National Service was completed in the Royal Air Force with the rank of Flying Officer.

He worked on the development and production of cathode-ray tubes with Ferranti Ltd. until 1960. The appointment as technical director of Electro High Vacuum was relinquished two and a half years later, when he joined Standard Telephones and Cables to lead the development on thin-film circuits.

Thick-Film Technology

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In recent years interest in so-called "thick films" has soared largely because of their potential low cost and because, in its simplicity, thick-film technology is closely related to standard printed-circuit practice. Thick films are deposited by screen printing, a process in which viscous pastes or inks are deposited through a patterned fine mesh screen onto a suitable ceramic substrate. Resistors, capacitors, inductors, and interconnections are deposited on alumina substrates in separate screenings using pastes of appropriate composition. The characteristics of the film are established by firing at an elevated temperature which also makes them integral with the substrate.

The technology can be employed in many applications since conductors, resistors, capacitors, and inductors as well as other functions can be produced in a variety of patterns over a wide range of values (Figure 1). To date, applications have been limited exclusively to the deposition of passive structures and networks, although a number of companies are now doing research in the screen printing of field-effect transistors and rectifying devices. By attaching active components to thick-film passive networks, thick-film hybrid microcircuits can be made. Present technology permits the fabrication of a variety of analog and large-signal or high-frequency digital circuits (small-signal, low- to medium-frequency digital circuits are more or less monopolized by silicon monolithics) [1, 2]. Thick-film and thin-film techniques are very often compared (rather unfairly for both). We believe that the two techniques are both viable and each has its useful range of applications. Thin films, for example, are prescribed for resistors and capacitors compatible with silicon-based microcircuits and have been widely used for precision resistance networks used in differential amplifiers, ladder networks, and digital-to-analog converters. On the other hand, thick-film technology is admirably suited for the mass fabrication of passive networks, for linear microcircuits, and large-signal digital modules.

Thick-film technology is intrinsically economical. Both original capital investment and operating costs are low. Processing equipment is developed and readily available, and production can be increased in relatively straightforward fashion once basic processes are established. The high yield and inherent versatility of the screen-printing process also contribute to the low operating costs. Artwork procedures are simple, so circuit modifications can be made merely by modifying stencil screen patterns and replacing the inexpensive screens on the production line. The processes are economical for short and long runs as well.

The high yields associated with thick-film hybrid microcircuits result from the ability to precisely adjust component values after firing, the ease of handling and machining ceramic substrates, the ability to completely test add-on components before connection, and the ability to batch-produce attachments using flow-soldering processes.

The best argument for thick-film circuits (and thin-film circuits) is the ability to batch-produce numerous connections in the manufacturing process, thereby eliminating the troublesome one-at-a-time welded or soldered connections.

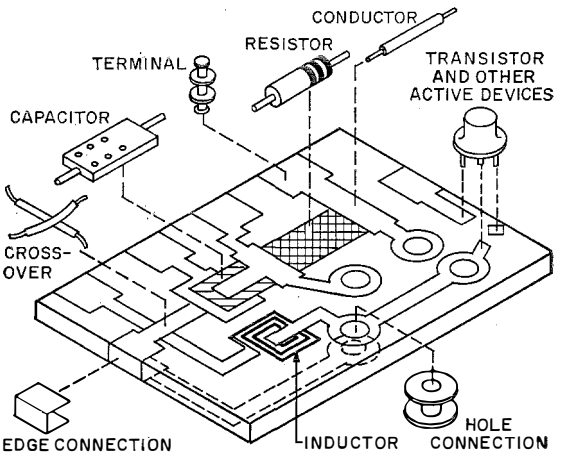


Figure 1—Functions performed by thick-film technology [1].

Due to the large commercial use of such circuits (which includes the recent use by International Business Machines of these techniques in a very large computer program involving ultimately millions of circuits), it is likely that thick films are here to stay, not only in the commercial field but also in space and military systems. For this reason they must be considered as an important segment of microelectronic technology.

An even more obvious trend is to place integrated silicon devices on ceramic wafers with thick-film components (and/or possibly thin-film ones) which cannot be economically fabricated in the silicon to provide a complete packaging system. This union of silicon and thick-film technology will provide a very practical, versatile, and economical tool for building electronic systems with a high degree of reliability.

1. Overall Processing

Figure 2 shows the steps involved in fabricating a typical thick-film hybrid microcircuit in which conductors,* resistors, capacitors, and inductors are screen printed, and leads and components are attached. This flow diagram represents maximum complexity. Circuits without capacitors, for example, require considerably fewer process steps.

The process is fundamentally sequential. The passive network is built in layers which are deposited and fired one after the other. Firing conditions are also reduced in staggered fashion to facilitate sequential fabrication.

* Edge connections and through-hole connections are formed during the deposition of the conductor layer. Insulating crossovers are deposited in a manner similar to capacitors.

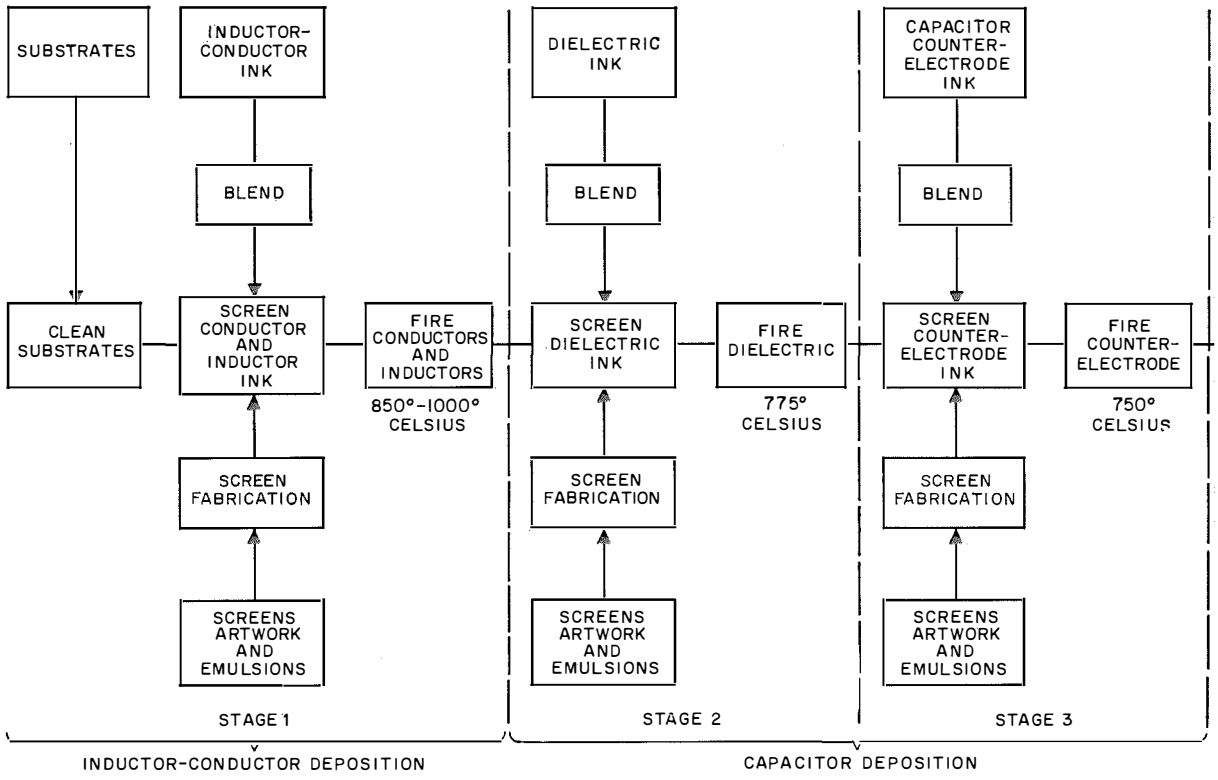


Figure 2—Thick-film hybrid microcircuit fabrication process.

At each stage of the fabrication cycle the same basic set of operations is repeated.

(A) A stainless-steel screen for selective deposition is prepared by standard photolithographic techniques.

(B) The appropriate ink is deposited on the substrate.

(C) The ink, after air drying, is fired at elevated temperature.

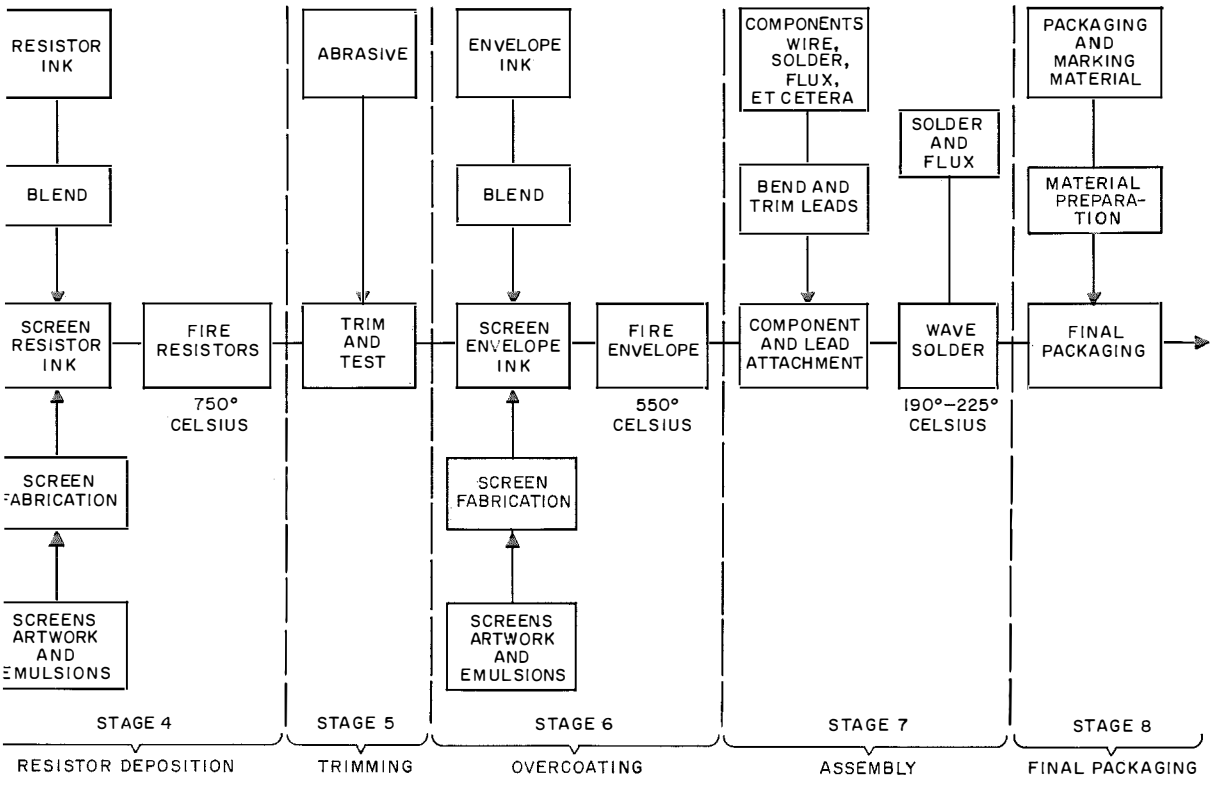
Inspection of Figure 2 demonstrates this cycle-within-a-cycle for stages 1 through 4. After the passive structures are formed, sandblasting or some similar technique is employed to trim the components to desired tolerance (stage 5). After abrasion, passive components are usually overcoated with a glaze or plastic encapsulant to enhance their environmental stability (stage 6). Leads and add-on components are attached and flow-soldered in place at stage 7. Final packaging (stage 8) completes the fabrication.

A circuit layout drawing is required to generate the artwork for screen fabrication. A typical layout is shown in Figure 3. A separate screen must be fabricated and used to deposit each circuit layer. Figure 4 shows a typical circuit at various stages of fabrication.

1.1 Inks (Pastes)

Just as the circuit requirements vary for each component (resistor, capacitor, et cetera), the formulation of the ink varies for the component to be deposited. A different screening composition is used for each type of component.

The ink contains the necessary polycrystalline solid ingredients to produce desired electrical characteristics; conductors have a high content



of metals or metal alloys, capacitors are high in dielectric, et cetera. In addition to the foregoing, a binder such as glass is added to bond the metallic or dielectric materials together and to the substrate. To meet the screening requirements, these ingredients are suspended in an organic carrier, such as butyl Cellosolve acetate, butyl Carbitol acetate, or terpineol.

It is important that the inks be well dispersed. Even at the high viscosity to which these inks are prepared, some settling occurs, the amount depending on the age of the ink as well as other history effects. To promote homogeneity the unopened ink jars should be placed on a slowly rotating jar mill. With newly received ink this helps to prevent settling and redisperses the solids, and with inks which have been opened and redispersed, it provides an excellent method of storage without fear of settling.

The ink must be stirred to uniform consistency before use. Usually hand stirring with a stainless-steel spatula will suffice. This stirring

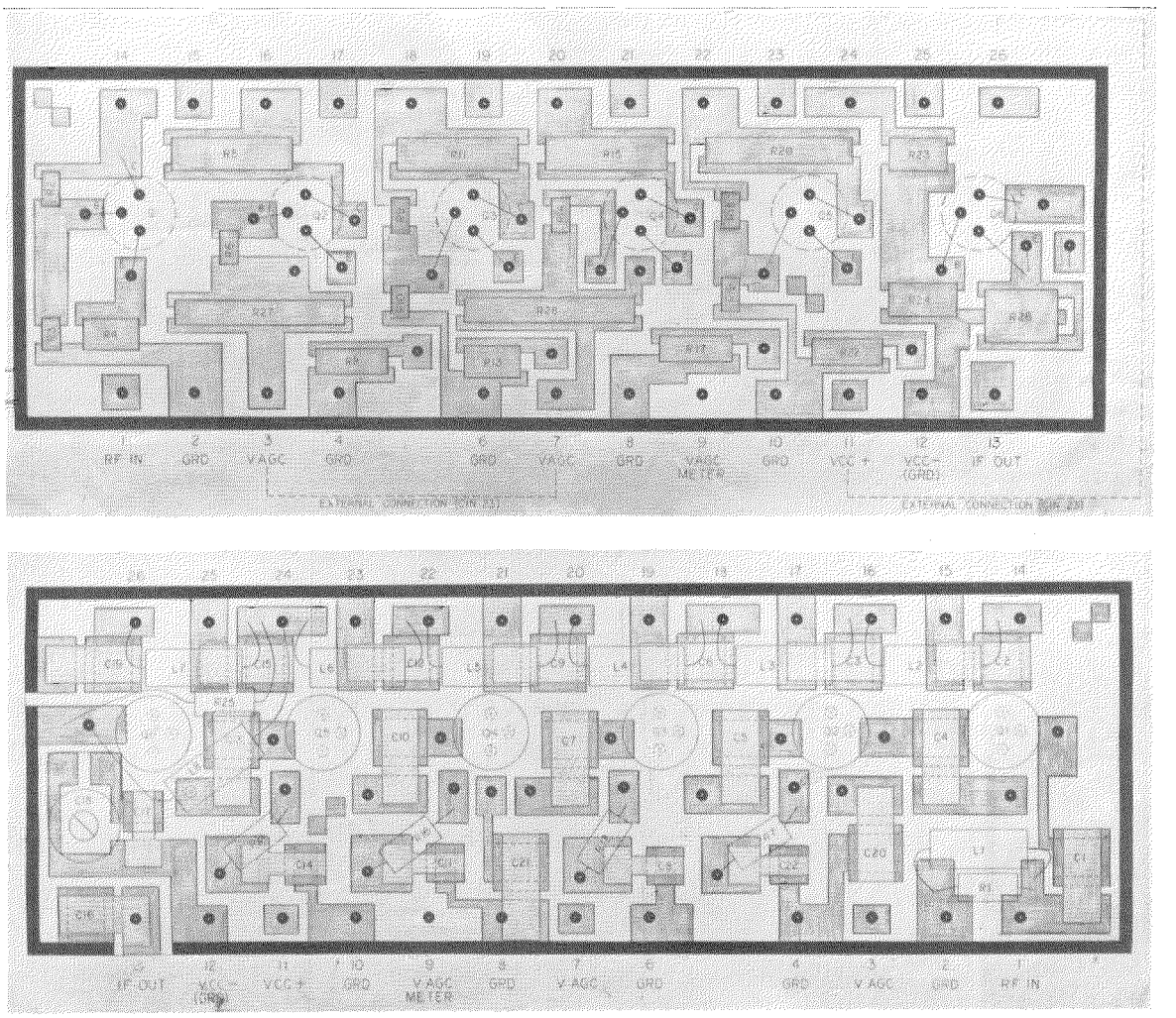


Figure 3—Thick-film hybrid microcircuit layout, showing both sides.

should continue until all sediment at the bottom of the jar has been dispersed and no lumps remain. Once the sediment has been at least partly dispersed by hand, a small laboratory stirring motor mounted on a ring stand with a blade device attached to the motor shaft can be used. If the solids are hardcaked at the bottom of the jar, it may be necessary to break up the cake, scrape it from the jar, and pass it through a 3-roll mill several times. This insures maximum dispersion but causes solvent loss. Solvent losses can be monitored by making periodic viscosity measurements. The Brookfield viscosimeter is commonly used for these measurements. The viscosities of commonly employed formulations average 2000 poises.

1.2 Screens and Screening

The screen is the means by which the ink is selectively deposited on the substrate. Screens are made from finely woven wire mesh, usually stainless steel, tightly stretched over and securely mounted to an aluminum frame. For most applications, a screen mesh size of 200 is quite satisfactory. In special applications, however, mesh sizes of 165 to 325 are used. The fine mesh sizes (high mesh number) tend to give thin deposits but fine line definition, whereas thicker deposits result from the coarser sizes (low mesh number).

The circuit pattern is generated on the screen by a photo-subtraction method. A photosensitive emulsion is applied to the screen, which when exposed through a photographic negative to ultraviolet light allows the circuit portion to be subtracted from the emulsion by simple washing. The development process leaves clear areas on the screen through which the ink can be deposited on the substrate.

Screens can be prepared in-house or purchased from outside vendors. In either case, a layout drawing is required from which photo-reduced working negatives are made.

Depending on the pattern accuracy required, master artwork may be prepared by tape-layout

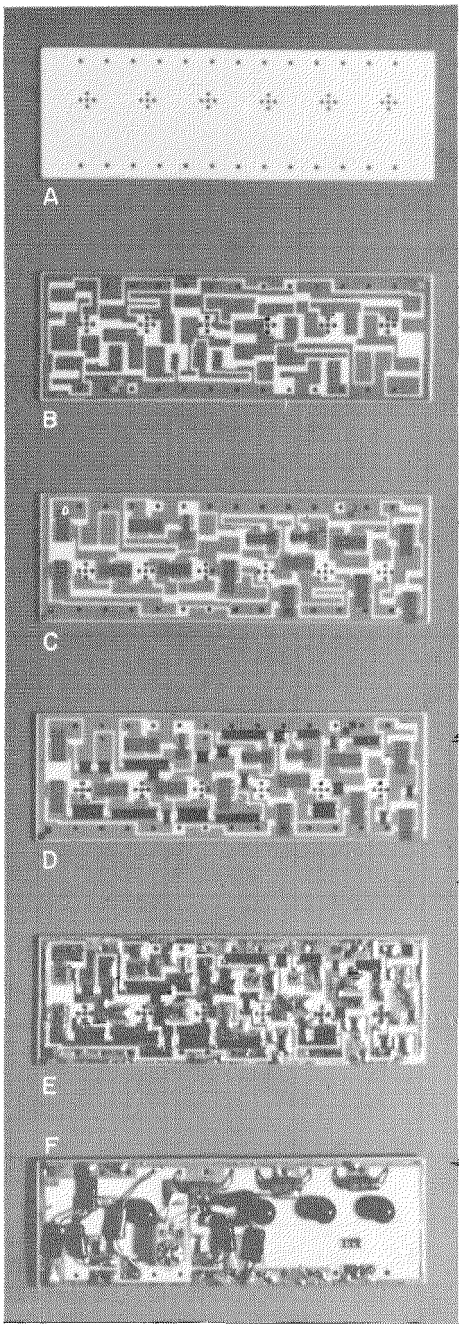


Figure 4—Typical thick-film circuit at various stages of fabrication. *A* is the 96-percent-alumina preformed substrate; *B, C,* and *D* show the addition of conductors, capacitors, and resistors, respectively; *E,* wave soldered; and *F* is the opposite side with add-on components and additional screen-printed conductors.

or coordinatograph (Figure 5). The master artwork is photographed by a reducing camera to furnish working photographic negatives (Figure 6).

Figure 3 shows a composite layout of a 70-megahertz 6-stage intermediate-frequency amplifier. Resistors and conductors are laid out on one side of the substrate while capacitors and additional interconnections are laid out on the other. While in Figure 3 all functions are presented together, separate interconnection, capacitor-dielectric, and resistor layouts as well as a sealant layout are required. The photolithographic process is repeated for each layer and a screen is prepared for each required deposition.

The processing of artwork and the preparation of screens is quite simple. Screens, for instance, can be completely processed in about 1 hour. Turnaround time for circuit changes can therefore be quite rapid.

1.3 Screen Printing Equipment

The screen printing equipment for producing hybrid microcircuits is designed to hold the screen, accurately position the substrate with reference to the screen, and squeegee the ink. Screening machines, both manually operated laboratory models and fully automated production models, are available from many manufacturers. Automatic machines can print several-thousand pieces per hour. Figure 7 shows a laboratory model while Figure 8 shows an automatic production machine.

To obtain uniform film thicknesses, control of the deposition of the ink is required. Processes are frequently designed around the convenient film thickness of about 1 mil.

The ability to print 1-mil films is determined by ink viscosity and by placing the screen at the correct distance from the substrate. Some latitude for variation does exist. If the screen is moved closer to the substrate, a thicker print results. Moving the screen away from the substrate reduces the thickness of the print. The optimum screening conditions are usually obtained empirically but, once obtained, are fixed with mechanical aids to ensure reproducibility.

1.4 Drying Equipment

Before the printed ink patterns undergo high-temperature firing, they must be dried following the removal of the screening vehicle. Drying may be accomplished by static heating in an oven or a suitable continuous-belt low-temperature drying oven.

1.5 Firing Furnaces

The most critical step in the preparation of thick-film circuits is the firing process. During

Figure 5—Artwork preparation on a coordinatograph.

Figure 6—Photo reduction.

this step the volatile materials completely evaporate, residual organics decompose, and the vitreous elements bind the formulation to the substrate. It is also the step where the characteristics of the components are permanently determined. Although static or hinge-type furnaces can be used to fire conductors or dielectrics, resistors produced by these means are very difficult to reproduce. Since complex physicochemical reactions are involved in the firing, exact reproduction of the firing cycle is required. This can best be accomplished in a continuous electric belt-type furnace in which temperature control of the center as well as the ends of the furnace hot-zone can be maintained. Belt speed control is also important, since the reaction of the formulation is in part controlled by the rate of temperature increase and decrease, as well as the time at peak temperature.

Like the screen printer and most other equipment required to produce thick-film circuits, a variety of belt furnaces is also readily available (Figure 9). These range from small laboratory models to large production models 50 feet (15 meters) long. The simplest furnace consists of nothing more than a belt, a temperature controller, and some heating elements, while the more-sophisticated ones contain gas curtains, ductwork to carry off the products of combustion, as well as belt-speed and heating-zone controls.

Although much work has been done to determine the effect of controlled atmospheres (oxygen, humidity concentration, et cetera) on the filmed circuits, no significant improvement has been found over the use of free flow of ordinary air.

1.6 Substrate Materials

The substrate material has a marked effect on the properties of the thick-film components [3]. Ceramics are the most suitable substrates, since they are among the only substrate materials capable of withstanding the firing temperatures (up to 1000 degrees Celsius) employed during

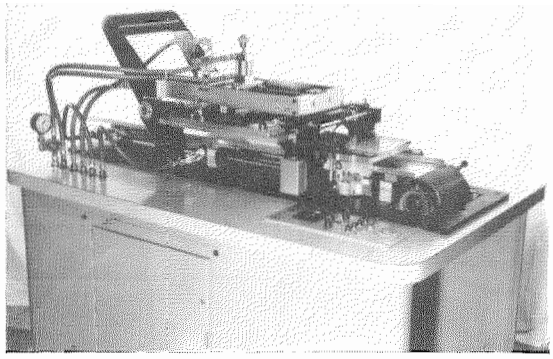


Figure 8—Automatic screen printer, production model.

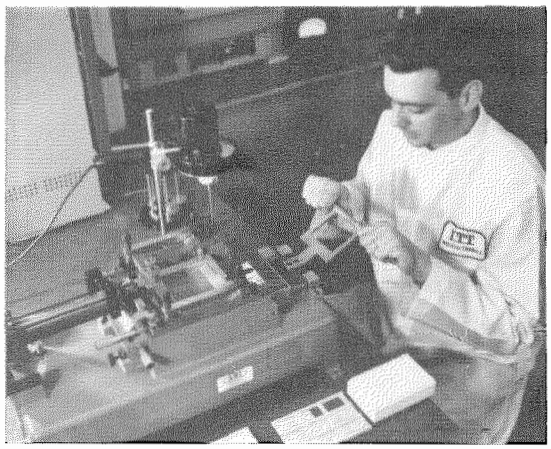


Figure 7—Semiautomatic screen printer, laboratory model.

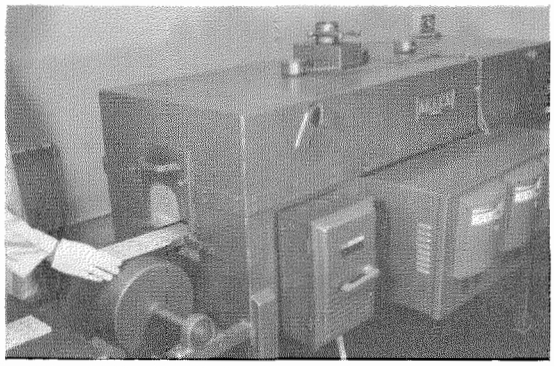


Figure 9—Furnace, production model.

thick-film processing. It is important that ceramic substrates be flat, smooth, and free of camber to provide the best possible reproducibility of thick-film components. The coefficient of thermal expansion of the substrate is also important, since it affects the temperature coefficients of resistors and capacitors by causing changes in particle-to-particle pressure when the components are heated.

The most widely used substrate material is 96-percent alumina. This material possesses a balance of physical and electrical properties which make it compatible with the resistor, capacitor, and conductor pastes commonly used. Other high-alumina bodies and other ceramics are available and also used, but in choosing the substrate, consideration must always be given to possible chemical effects. The same component ink deposited on different substrates, or on two varieties of the same nominal substrate, may exhibit markedly different characteristics. The properties of a number of substrate materials are summarized in Table 1.

1.7 Conductors

Conductor inks are based primarily on metal-glass mixtures. Compositions containing palladium-silver, gold-platinum, silver, or platinum are available. The conductor inks are sufficiently low in resistivity to be used as interconnections for the resistors, capacitors, solder pads, and any "add-on" components such as diodes, transistors, et cetera, that may be required. The "fired-on" conductors can be soldered, welded, or thermocompression bonded without difficulty. In addition to the above, both sides and the edges, as well as through-holes in a substrate, can be metallized with screened deposited conductor inks.

The conductor formulations consist of a finely divided suspension of metal powders and glass in an organic vehicle added to make the ink screenable. After proper drying and firing, the ink forms a matrix of metal particles in glass, with the glass binding the agglomerate to the substrate.

TABLE 1
Ceramics Suitable for Thick-Film Technology

	Substrate Material						
	Aluminum Oxide (96 percent)	Forsterite	Beryllia	Titanium Dioxide	Steatite High Expansion	Steatite Low Expansion	Typical Resistor Composition
Linear thermal coefficient of expansion per degree Celsius (25–900 degrees Celsius)	7.9×10^{-6}	11.7×10^{-6}	8.5×10^{-6}	9×10^{-6} (25–700 degrees Celsius)	9.6×10^{-6}	8×10^{-6}	7.6 to 8.2 $\times 10^{-6}$
Thermal conductivity at 300 degrees Celsius (gram-calories per second per square centimeter per degree Celsius)	0.041	0.008	0.28	0.012	0.006	0.006	—
Dielectric constant (at 1 megahertz and 25 degrees Celsius)	9.1	6.2	6.4	85	6.0	6.3	—
Water absorption (percent)	0	0	0	0	0 to 1	0	—
Continuous operating temperature (degrees Celsius)	1550	1000	1000	1600	1000	1000	—
Volume resistivity (ohm-centimeters at 25 degrees Celsius)	10^{14}	10^{14}	10^{14}	10^{12}	10^{14}	10^{14}	—

Two-hundred-mesh screens are usually employed to deposit conductors. Where narrow conductor paths are required (5 mils or less), a finer mesh size of 270 to 325 may be required to obtain the required definition. After screening, the solvents are evaporated by heating to 100 degrees Celsius for about 15 minutes. Where continuous operation is desired, a bank of infrared heat lamps or a low-temperature belt furnace can be used to dry the ink just before high-temperature firing. This automatic drying can, of course, be used with any printed deposit.

The firing cycle should be designed to optimize the conductivity, adhesion, and solderability of the conductor. Firing temperatures range from 500 to over 1000 degrees Celsius, depending on the ink used and the final application of the conductor.

Of the conductor compositions available from du Pont, the gold-platinum ink is preferred over the other conductor inks because, in general, it is the most versatile and easiest to process.* This ink may be fired over a temperature range from 760 to 1025 degrees Celsius, with firing times of 5 minutes to 1 hour being reported. This makes for considerable process design freedom.

At the lower end of the temperature range, the conductor can be co-fired with the resistor inks, but adhesion and solderability are sacrificed. At the higher end of the temperature range, it must be screened and fired first, followed by the resistor screening and firing. Adhesion in the latter case is around 1500 pounds per square inch (105 kilograms per square centimeter) and some reports indicate a strength almost 3 times greater [3, 4]. Resistivity is about 0.1 to 0.01 ohm per square mil and can be decreased to about $\frac{1}{10}$ this value by applying solder over the conductor [3].

Silver inks can be used for conductors, but in the presence of a direct-current potential and high humidity the silver can migrate between closely spaced conductors, producing shorts [5]. When silver inks are used as resistor terminations, the resistor ink is screened and fired first followed by the silver conductor, which is then fired at 540 degrees Celsius. Solderability is good but the solder should contain about 2- to 3-percent silver to minimize the alloying of the silver conductor with the tin in conventional solder.

Gold is also used as a conductor material, but it also readily alloys with solder. It is used frequently as a capacitor counterelectrode. The gold can be overcoated with glass to prevent alloying with the solder.

Since the resistors and capacitors (Sections 1.9 and 1.10) are fired at temperatures in excess of 700 degrees Celsius, the application of solder to the conductor is performed as a final step. This can be accomplished by wave or dip soldering the entire circuit. The operation has little or no effect on the characteristics of the fired components. The conductor, however, contains noble metals which can alloy with tin-bearing solders. As a consequence, solder coating should be performed rapidly to limit the exposure of the conductors to possible alloying species. Commercially available solders, such as 60-percent tin and 40-percent lead; 62-percent tin, 36-percent lead, and 2-percent silver; 10-percent tin and 90-percent lead; may all be used successfully with commonly employed thick-film conductors.

1.8 Inductors

Inductors in thick-film technology are obtained by printing spiral or linear patterns (depending on frequency) of conductor ink on the substrate. To optimize inductor Q, the conductivity of the patterns is enhanced by solder coating or electroplating. Even so, Q's seldom exceed 100. Using spiral patterns and 0.005-inch (0.002-centimeter) conductor widths, inductances of the order of 1 to 900 nanohenries can be obtained. Use of ferrite coupling between conductors will increase values approximately 5-fold.

*Recently du Pont has released a palladium-gold composition which is alleged to provide characteristics equal to or better than platinum-gold and at much lower cost.

Such inductors are useful only above 10 megahertz. At lower frequencies, printed inductors take up more substrate surface area than they are worth, and the use of discrete microminiature inductors below 10 megahertz is more or less standard practice.

1.9 Resistors

Reliable and reproducible resistors are made by the same screening techniques used to produce thick-film conductors and inductors [6, 7, 8].

Most industrial users employ resistor compositions supplied by E. I. du Pont. Du Pont resistor inks are high-viscosity mixtures of precious metals or precious-metal oxides and vitreous binder, all suspended in an organic vehicle. The nominal characteristics of typical materials are printed in Table 2.

These data were obtained by du Pont by screen printing the resistor inks and firing in a continuous furnace at a belt temperature of 1350 degrees Fahrenheit (732 degrees Celsius). The *8000*-series compositions were calibrated on 96-percent alumina.

The *7800* series is based on palladium oxide, while the *8000* series is based on palladium-silver. In each series the percentage composition of glass determines the nominal resistance in ohms per square per mil.

Figure 10 shows the general firing characteristics of the two resistor inks. While such du Pont data are useful for orientation, the exact behavior of the various inks must be determined experimentally in the complex manufacturing environment (as a function of ink blending, printing procedure, firing cycle, belt speed, et cetera). The task of characterizing inks is relatively straightforward, not nearly as formidable as it might appear. Approximate firing temperatures for inks used by ITT Federal Laboratories are shown in Figure 2.

The *7800* series is less sensitive to firing conditions than the *8000* series and is probably to be preferred to the latter because it provides equal electrical performance at lower cost. The *8000* series offers a much wider range of available resistance, though to guarantee close resistor reproducibility it requires closer control over screening and firing processes. The batch-

TABLE 2

Characteristics of Thick-Film Resistor Materials

Resistor Composition	Nominal Resistance (ohms per square per mil) on Alumina	Temperature Coefficient of Resistance (parts per million per degree Celsius)		Noise (decibels per decade)	Drift (percent)
		(25 to 105 degrees Celsius)	(25 to 75 degrees Celsius)		
7826	125	+740*	—	−20	0.10†
7827	1000	+500*	—	−23	0.17†
7828	2500	+245*	—	−13	0.10†
7832	6250	+265*	—	+ 3	∼0.10†
448–7022R‡	50	+225*	—	−25	∼0.10†
448–7023R‡	500	+225*	—	−25	∼0.10†
448–7037R‡	15 000	+225*	—	+ 5	∼0.10†
8020	1	+300	−250	−35	1.0§
8025	20 000	− 50	+300	+15	1.0§

* 25 to 125 degrees Celsius.
† After 1000 hours at 85 degrees Celsius, no load.
‡ New 7800 series inks.
§ After 1000 hours at 150 degrees Celsius, no load.

to-batch reproducibility of the *7800* series is presently better than that of the *8000* series.

Optimum resistor characteristics (temperature coefficient of resistance, drift, range, et cetera) are obtained by blending the basic mixtures within a given series to form a functional mixture of intermediate resistance.

With the *8000* series, a resistance of about 3000 to 5000 ohms per square per mil provides an excellent balance of characteristics and a suitable range of resistance values.

Very low resistance inks tend to exhibit large temperature coefficients of resistance and drifts because of the low-percentage composition of glass which acts as binder and particle encapsulant. Very high resistance inks show better drift and temperature coefficient of resistance behavior but are difficult to reproduce.

From a design point of view, thick-film resistors prepared from simple blends of currently available resistor inks offer the excellent range of characteristics shown in Table 3.

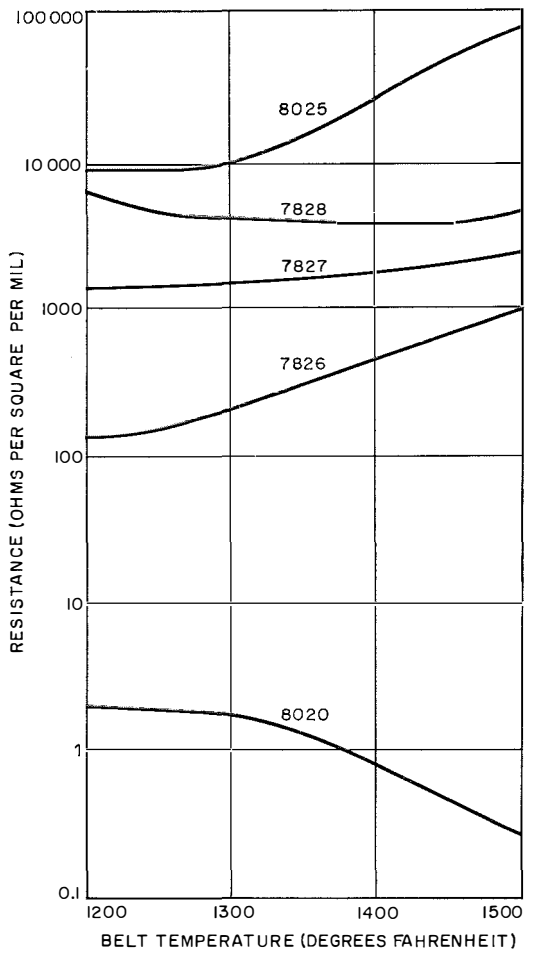


Figure 10—Resistor firing characteristics. The numbers on the curves represent resistor compositions.

TABLE 3

SUMMARY OF THICK-FILM RESISTOR CHARACTERISTICS

Resistivity (ohms per square per mil)	1–400 000
Resistance range (ohms)	$10–10^6$
Temperature coefficient of resistance (parts per million per degree Celsius)	±50–±300
Roll-off frequency (gigahertz)	1–2
Tolerance:	
Percent with trimming	0.025
Percent as fired	5
Drift at 150 degrees Celsius (percent per 1000 hours)	0.5

The realization and reproducibility of useful resistor results are in large measure empirical and a matter of technique.

Thick-film techniques are suitable for laboratory, pilot, or large-scale production, and the ability to realize the above range of characteristics is largely a matter of in-house skill.

While the du Pont mixtures are widely used, many companies are conducting their own materials projects with improved electrical characteristics or lower-cost systems based on nonprecious metals or compounds [9, 10]. International Business Machines has already reported the in-house development of a resistor system based on indium oxide [11].

The "as fired" resistors consist of a matrix of metal oxide and metal alloys encased in glass which effectively forms an envelope excluding most contaminants. In practice, it would be desirable to use this hermetic glass-sealed structure directly but this is not always possible. If tolerances of 10 percent or poorer are permitted,

the resistors can be used without adjustment or any protective coating. However, many applications require closer tolerances. Here the resistors must be trimmed to the correct value. Trimming is achieved by removing resistor material, thereby decreasing the effective cross-sectional area, yielding higher resistance. Many techniques are used to trim resistors—spark erosion, diamond wheel scribing, and air-abrasive trimming, to mention a few in current use. Probably the most widely used method is air-abrasive trimming. In this technique a fine abrasive powder, air-propelled through a jet nozzle, is directed at the edge of the resistor and removes some of the material, thereby adjusting the resistance to higher values. This technique lends itself readily to automation. Several nozzles can be arranged to trim more than one resistor at a time. When coupled to automatic monitoring equipment, such an arrangement permits very rapid efficient trimming. It should be noted that the cost of trimming varies directly with the tolerance requirement. Close tolerances are expensive.

While abrasive trimming is quite effective, the process opens the resistor surface and exposes the interior to deleterious environmental effects. Trimmed resistors must be resealed by overcoating them with glass or resin encapsulants.

1.10 Capacitors

Many fabricators of thick-film circuits restrict their activities to the production of resistor networks. Thick-film capacitors can also be made by screen printing dielectric inks. Until recently, most thick-film fabricators developed their own proprietary dielectric formulations. Screenable dielectric formulations have just become available commercially [12].

The structure of a thick-film capacitor consists of a printed dielectric layer between two printed conductors. Figure 11 shows a typical structure. Higher capacitance per unit area can be obtained by paralleling such structures. Printed capacitors are invariably overcoated (usually with glass) for environmental protection and to protect the counterelectrode from solder-alloying.

As with other types of thick-film inks, dielectric formulations are mixtures of glass frit, organic vehicle, and, in this case, a suitable dielectric powder. A number of papers have been published on thick-film capacitors, but at the present state of the art thick-film capacitors are of three general classes and are based in the main on these dielectrics: barium titanate, titanium dioxide, or borosilicate glass frit.

Barium titanate-based capacitors offer high capacitance per unit area, (8000 picofarads per square centimeter per mil). They tend to get lossy at high frequencies ($Q = 25$ at 70 megahertz) and are useful as blocking or bypass capacitors.

Titanium-dioxide capacitors offer somewhat less capacitance per unit area (3000 picofarads per square centimeter per mil), show reasonably high Q's up to 500 megahertz, and are excellent for tuning applications.

A third class of capacitor application, that of the lead crossovers, is performed by using screened glass frit between metal lead intersections. A number of crossover formulations are available which provide excellent lead insulation and show parallel capacitance as low as 0.5 picofarad [12].

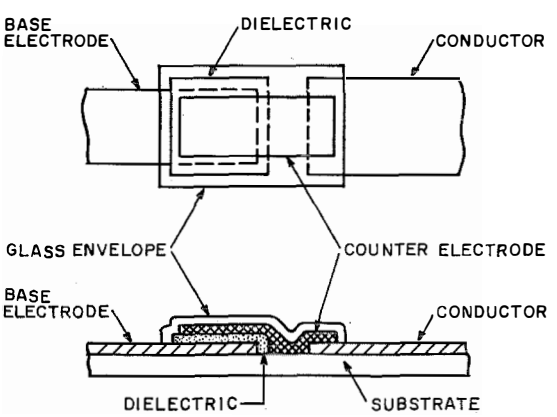


Figure 11—Thick-film capacitor structure.

Thick-film capacitors of all three categories show excellent voltage-breakdown behavior. Voltage breakdown consistently exceeds 500 volts per mil. Pinholing and leakage are no problems with thick-film capacitors. Their design characteristics are summarized in Table 4. Like resistors, capacitors can be air-abrasively trimmed to close tolerances.

TABLE 4
SUMMARY OF THICK-FILM CAPACITOR CHARACTERISTICS

	Barium Titanate	Titanium Dioxide	Crossovers
Capacitance per unit area (picofarads per square centimeter per mil)	8000	3000	135
Capacitance range (picofarads)	100–10 000	10–1000	0.5–1.0
Tolerance:			
Percent as fired	10–20	10–20	20
Percent with trimming	1	1	Not applicable
Temperature coefficient of capacitance (parts per million per degree Celsius)	1000	200	1000
Voltage breakdown (volts per mil)	>500	>500	>1000
Q:			
100 kilohertz	100	>200	150
70 megahertz	25	100	100
Drift	relatively stable	stable	stable

2. Applications of Thick Films

Thick-film applications can be broadly divided into two classes: passive networks (discrete thick-film resistors are included in this class), and thick-film hybrid microcircuits.

2.1 Passive Networks

Tens of millions of resistor and resistor-capacitor networks have been produced during the last decade and are in widespread use in commercial, industrial, and military equipments. In passive-network applications the design usually stresses the low-cost high-volume production characteristics of thick-film technology. The major advantage of thick-film networks is the ability to simultaneously batch-produce interconnections, thereby eliminating troublesome one-at-a-time welded or soldered connections. Figure 12 shows examples of thick-film passive networks which are direct replacements for discrete component assemblies. The wide range of passive-component characteristics available give the designer virtually limitless freedom.

2.2 Hybrid Microcircuits

The attachment of discrete active components to thick-film substrates also permits the fabrication of a variety of digital, linear, and pulse circuits, which will operate over the frequency

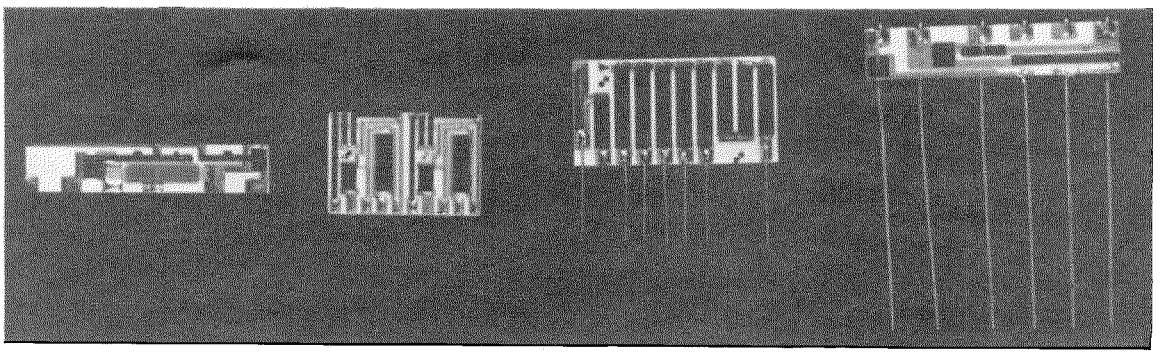


Figure 12—Thick-film passive networks.

range from direct current to 500 megahertz. In most cases, thick-film microcircuits can be made by direct translation from their discrete lumped-component predecessors. Again design freedom is virtually limitless [13, 14, 15].

Aside from the small-signal digital application of thick films in the International Business Machines series-*360* computers, most thick films have been employed in digital interface and linear circuits. By way of example, International Telephone and Telegraph Corporation has designed and produced a microminiature 8-gigahertz microwave terminal in which all circuits operating below 150 megahertz are constructed using thick-film technology. All radio-frequency functions of the microwave terminal shown in Figure 13 are modularized, and each of 22 plug-in modules is constructed as shown in Figure 14 (a 70-megahertz intermediate-frequency amplifier complete with automatic gain control).

Figure 15 shows the assembled thick-film substrate which goes into the 70-megahertz intermediate-frequency strip. It has 21 capacitors deposited on the transistor side and 23 resistors printed on the reverse side, shown mirrored. From this degree of complexity, it is quite obvious that thick-film technology offers a versatile tool to the circuit designer.

We are presently doing work which will extend the usefulness of thick-film components and techniques into the gigahertz frequency range, performing materials studies to improve component characteristics, and actively building circuits which combine silicon linear integrated circuits and thick-film resistance-capacitance-inductance networks.

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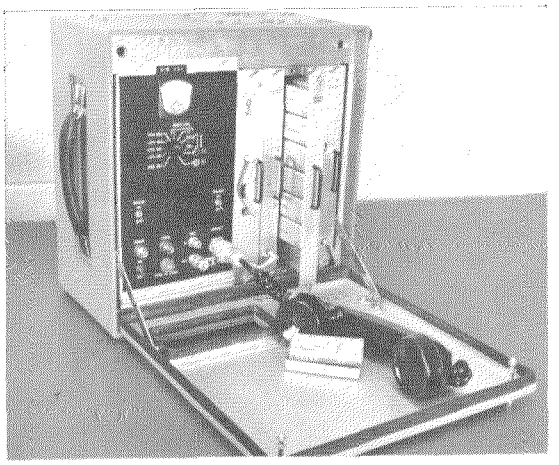

Figure 13—Microelectronic (thick-film) microwave terminal.

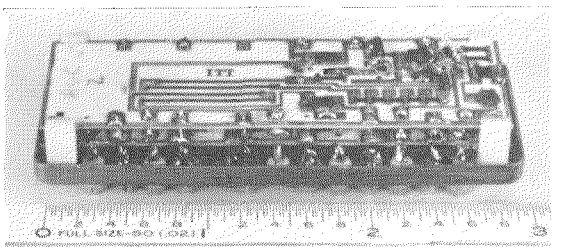

Figure 14—Thick-film module, 70-megahertz intermediate-frequency amplifier.

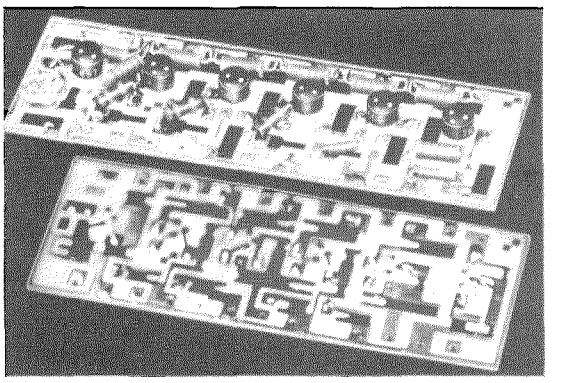

Figure 15—Thick-film assembly, 70-megahertz intermediate-frequency amplifier.

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From 1957 to 1960 he served as a staff chemist for the product development laboratory of International Business Machines. For the next three years, he was with General Telephone and Electronics Laboratories. In 1963 and 1964 he was director of the chemical laboratory of Republic Aviation Corporation.

In late 1964 Dr. O'Connell joined ITT Federal Laboratories and is now manager of its Microelectronics Department.

He holds membership in the American Chemical Society, Electrochemical Society, and the Institute of Electrical and Electronics Engineers.

Edwin A. Zaratkiewicz was born in Passaic, New Jersey, on 20 October 1922. After serving

with the United States Marine Corps from 1942 to 1946, he received a bachelor's degree cum laude in physics from Fairleigh Dickinson University in 1955.

He joined ITT Federal Laboratories in 1950 and worked extensively on rectifier and transistor junctions and on both thin-film and thick-film technologies. He is now a section head in the Microelectronics Department.

Mr. Zaratkiewicz is a member of the Institute of Electrical and Electronics Engineers and of the American Physical Society.

Deloraine Receives First Award in International Communication

E. Maurice Deloraine received the initial Award in International Communication conferred by the Institute of Electrical and Electronics Engineers, "in consideration of his outstanding technical and scientific contributions in the field of international communications extending over a period of more than 45 years, and particularly for his active leadership in many fields of communication in Europe and in the United States of America."

The award was established through agreement between the Institute of Electrical and Electronics Engineers and the International Telephone and Telegraph Corporation in memory of Hernand and Sosthenes Behn, the founders of the corporation.

E. Maurice Deloraine was born in Paris in 1898. He received the diploma of Physicist from the School of Physics and Chemistry and the degree of Docteur-Ingenieur from Paris University.

After service in the French Army Signal Corps, he joined the London engineering staff of the International Western Electric Company in 1921. He worked on radio broadcast transmitters and was responsible for part of the development in Great Britain of the first transatlantic radiotelephone circuit.

In 1928, after acquisition of International Western Electric by International Telephone and Telegraph Corporation, he organized its Paris laboratory, Laboratoire Central de Télécommunications, where under his direction pulse-code- and pulse-time-modulation techniques were invented and perfected. He contributed importantly to ultra-high-frequency communications and to high-power broadcasting and television.

Dr. Deloraine was transferred to the United States in 1941 and established a laboratory for defense work. In 1946 he became general technical director and was personally active in research and development of switching systems. Later he served as president of the System subsidiaries in France. Now retired from active service, he continues as director of several of the French companies.

He was made a Chevalier of the Legion of Honor in 1938 for exceptional services to the Posts and Telegraphs Department of France and in 1945 was promoted to an Officer of that Legion by the Minister of the French Navy. In 1963 he was made an Officer of Postal Merit and the next year Commander in the National Order of Merit by the Minister of Posts and Telecommunications. In 1966 he received the order of Commander of Merit from the Italian republic.

Dr. Deloraine is a Fellow of the Institute of Electrical and Electronics Engineers and a Member of the Institution of Electrical Engineers in Great Britain. He holds membership in several scientific societies in France.

Interconnections for High-Density Packaging

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ITT Europe; Brussels, Belgium

1. Factors Affecting Packing Density

1.1 Component Sizes

Consider first the actual space occupied by various types of circuit assembly. Figure 1 dramatically illustrates what has been achieved by the new microelectronic techniques. In the case of semiconductor integrated circuits, it can be seen that even the most modern encapsulations are large compared with the semiconductor chip itself and that the theoretical limit in packing density has not been reached even with advanced devices such as integrated circuits in packaged form. The dominant size factors are encapsulation, associated wiring, and components (such as inductors) not capable of comparable miniaturization.

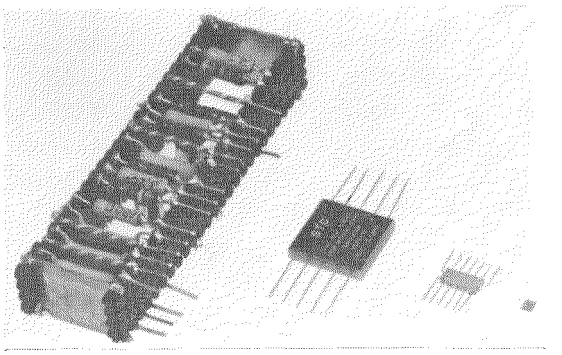

Figure 1—The relative sizes of assemblies of conventional components, thin-film circuits, packaged semiconductor integrated circuits, and semiconductor chips indicate the potential for miniaturization and the handling and interconnection considerations.

The size and complexity of circuit cards for integrated circuits are dictated largely by the field of application. In general, digital systems can make maximum use of the various forms of integrated circuit, and relatively high packing density can be achieved. The main limitations encountered result from the complex interconnection field required, the ability to provide sufficiently dense plug-in connector fields, and the control of heat dissipation. In digital circuits associated with electromechanical devices such as relays, and in linear systems where such components as inductors and filters dominate, the bulky associated components limit the density that can be achieved.

The subrack, which in many types of static equipment may house up to 50 circuit cards, is an important size limiting factor. The limits are set by the complexity of the interconnections and the allowable heat dissipation of the equipment. To illustrate the density of interconnection encountered, Figure 2 shows the subrack wiring of a typical unit used in an electronic switching system designed with conventional components.

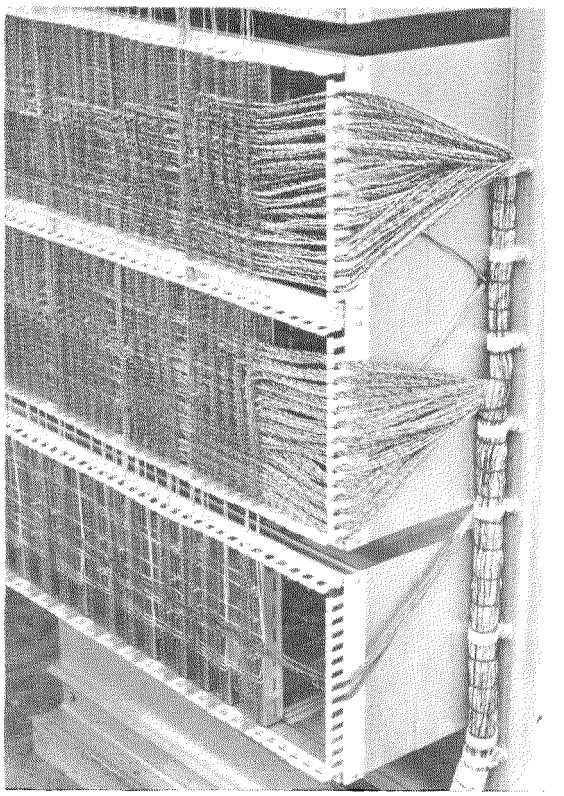

Figure 2—The density of back-wiring required with conventional components is already a problem. Compressions of 10 to 100 times will make this problem very severe.

Using semiconductor integrated circuits, packing densities of 10 to 100 times greater than

is usual with conventional components can be attained. For example, an *ISEP* subrack [1] approximately 5 × 5 × 20 inches (12·7 × 12·7 × 50·8 centimetres) in size can accommodate without difficulty about 1800 semiconductor integrated circuits—the equivalent of about 40 000 conventional components. With such packing densities the back-wiring problem, already severe, becomes extremely difficult.

In the case of mobile, airborne, or aerospace equipment, different considerations apply. In general, the equipment must be more compact but fewer external connections are required. Even in this type of equipment, however, it has not yet been practical to exploit the miniaturization potential of integrated circuits to the full.

1.2 Reliability

It is generally accepted that the various forms of integrated circuits are extremely reliable and that the mounting and interconnection methods and general equipment design should not significantly degrade this reliability. The intrinsic reliability of the integrated circuits themselves depends largely on minimizing interconnection interfaces and making necessary connections under carefully controlled conditions. The leads, being short, are insensitive to vibration. These criteria can form useful guide lines in the development of general interconnection techniques for maximum reliability.

The application of the new techniques increases the heat dissipation per unit volume; dissipation, being largely controlled by considerations of operating speed and noise sensitivity in both analogue and digital circuits, cannot usually be reduced in the same ratio as the volume. Thus, either some of the potential reliability increase must be sacrificed by working at higher temperatures, or forced cooling must be applied. This introduces the further problem of the reliability of the cooling equipment itself.

Decrease of size also increases the difficulty of securing adequate reliability from both permanent and plugged connections.

Soldering is still used most widely for permanent connections, and if the process is in good manufacturing control, reliability can be satisfactory. It has the advantages of low cost and ease of repair. Under arduous environmental conditions it is less reliable than welding, and difficulties are often experienced if it is used for making small closely grouped joints. Improved reliability is being sought through the use of refined soldering techniques based on microwelding practice. Pre-tinned parts or solder preforms are fused using electrode arrangements similar to those used for welding. Thus accurate control of time, temperature, and position is achieved.

Resistance and percussive-arc welding are widely used for interconnection of integrated circuits, particularly where requirements call for small size and resistance to adverse environmental conditions. A programmed welding machine must be used to compete in cost with flow-soldering, and very close process control is necessary to ensure good reliability.

Connectors are important when considering reliability and cost. The aim is to have as few as possible for maximum reliability, but maintenance needs usually dictate the number required for any given application. With the increased use of integrated circuits, smaller connectors are required if full advantage is to be taken of the improved packing density made possible. Reliable miniature connectors are at present costly and require more-careful handling than conventional connectors.

1.3 Cost Considerations

In most of the potential applications of integrated circuits, cost and reliability are—as already stated—more important than reduced size. Thus the most important advantages of the integrated circuits themselves are not primarily related to their smallness. To secure the minimum total equipment cost for a given type of application, it is therefore necessary to take account of the factors discussed in Sections 1.1 and 1.2.

It is clear that excessive miniaturization can increase costs and reduce reliability. The mere assembling of components in a compact manner is not particularly difficult; the important problem is to find practical and economic ways of interconnecting them.

2. Interconnection Topology

2.1 Single-Plane Interconnections

Until a few years ago, single-sided printed-circuit boards provided adequate facilities for interconnecting 2-lead or multi-lead components on plug-in cards. With increasing use of multi-lead packages and increasing packing density, 2-layer and multi-layer boards have come into use. In a discussion of interconnection topology, it is necessary to distinguish between theoretical problems and practical problems. The main question is—what are the theoretical limitations of a single-plane system of interconnections?

Figure 3*A* represents the wiring side of a printed-circuit card, all the components being on the reverse side. The points *a, b, c,* et cetera, are the terminals on the components. Suppose that a certain number of connections have been made successfully in the one plane. If the next connection to be made is from terminal *r* to terminal *s,* then (ignoring for the moment any consideration of the shortest physical path) we can proceed as follows.

Starting from *r* move towards *s* until an obstacle is encountered, for example as shown at 1. Skirt around the obstacle until it is again possible to move towards *s* as indicated at 2. Repeat the process with successive obstacles as shown, for example, at 3 and 4 until *s* is reached.

The process described fails if any obstacle encountered consists of a closed loop with *r* inside and *s* outside or vice versa. But electrically a closed loop is never needed, since all the terminals connected by such a loop remain connected if the loop is broken at any one point. Thus all closed loops can be eliminated and the process will always succeed.

Extension of the reasoning to include the interconnection of any number of terminals by one track is trivial.

Finally, since the connection *r–s* can be made in the presence of any number of previous connections, it must be possible to repeat the process for the remaining connections until the circuit is complete.

Figure 3*B* shows a case with some connections made to points on the edges of a board, for example, to a plug or to test points. Such connections do not invalidate the principle provided that no track is connected to two points on the edges. For example, a connection such as *t–u* from a plug-in point on the back of a board to a test point on the front forms a loop with the edge of the board, so that a connection such as *v–w* cannot be made. There appear to be no significant theoretical limitations to planar layouts.

However, there are two basic practical difficulties: Firstly, the theoretical solution may need more printed-circuit tracks passing between certain pairs of terminals than are compatible with reasonable terminal spacing and track spacing. Secondly, the long tracks needed may be electrically intolerable.

A further difficulty is the enormous amount of trial and error involved in examining the interconnection possibilities in practical cases. Up till now this difficulty has prevented a logical assessment of the stage at which the practical

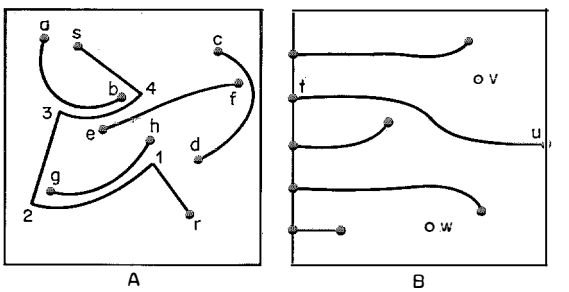

Figure 3—Single-plane connections have no important theoretical limitations. However, the practical limitations are severe.

problems of single-layer interconnections necessitate the use of more layers. The application of computers to this problem should clarify it.

2.2 Two-Plane Interconnections

A typical 2-plane system is a double-sided printed circuit with through-connections from one plane to the other wherever required. It is obvious that there can be no significant theoretical limitations since there are almost none for a single-plane system.

The practical limitations are far less. The essential difference between a 2-plane system and a 1-plane system is that in finding a path from one point to another it is unnecessary to skirt around previously made connections, since an obstacle can always be by-passed by transferring to the other side of the plate via a through-connection.

Thus it is relatively easy to provide short connections. In consequence, with a given track pitch, a smaller total area is required for interconnections. Furthermore there will generally be a number of alternative paths for a given connection, not differing much in length, so that the need to cross restricted regions can be relatively easily avoided. In any case, a double-sided system will always permit twice as many connections in any particular region as a single-sided one.

The usual way of applying 2-plane connections to the interconnection of integrated circuits is to distribute the packages uniformly over the board and interconnect by tracks running between and, where practicable, underneath the packages. The packing density attainable depends on the circuit complexity, the minimum track spacing, and the package terminal layout. Given the general class of circuit, the track spacing, and the package type, the layout of arrangements of this sort can be divided into two phases. Firstly, the determination once and for all of the general arrangement for that class (package pitch, number of tracks between packages, et cetera) which will permit solution of a sufficient number of circuit problems to allow useful design and manufacturing standardization. Secondly, the design of particular circuits in terms of the predetermined standards. The determination of optimum arrangements in both stages is a good field for computer-aided design.

In practice, an elementary trial-and-error process is not feasible unless the number of packages per unit is very small or the class of circuit is simple. For example, for 20 packages on a card (a very moderate number) a complete trial-and-error approach requires calculating the optimum wiring pattern for each possible arrangement of packages, and then selecting the best package arrangement and best interconnection pattern for that arrangement. The number of ways of arranging 20 packages in 20 defined positions is factorial 20 which is roughly $2{\cdot}5 \times 10^{18}$. Allowing only 1 microsecond for each trial, the total time becomes roughly 10^5 years.

Another approach, starting from basic topological considerations, is illustrated in Figure 4*A*. Here all the terminals to be interconnected (T_1–T_{n1}) are arranged in a column. These terminals will, in general, be grouped on multi-terminal packages or components P_1, P_2, et cetera. Suppose that a horizontal conducting track is connected to each terminal. Then any system of interconnections between the terminals can be built up by means of vertical tracks V_1 to V_{n2} insulated from the horizontal tracks except for appropriate cross-point connections.

It is obvious that the number of vertical tracks needed cannot exceed the number of horizontal tracks. If there is one vertical track for every horizontal track then every horizontal track can be connected to a vertical track at one point. The vertical track will then cross all other horizontal tracks and any system of connections whatsoever can be made.

In practice, the number of vertical tracks needed is always much fewer than the number of horizontal tracks. Logic circuits present the most difficult problem. In this case the units

P_1, P_2, et cetera, will be characterized by having one or more outputs and a greater number of inputs, and the interconnections will consist of each output being connected to a number of inputs. Thus if each output terminal (typically, one-fifth of the total number) is connected to a vertical track by a cross-point connection, any combination of connections from outputs to inputs can be achieved.

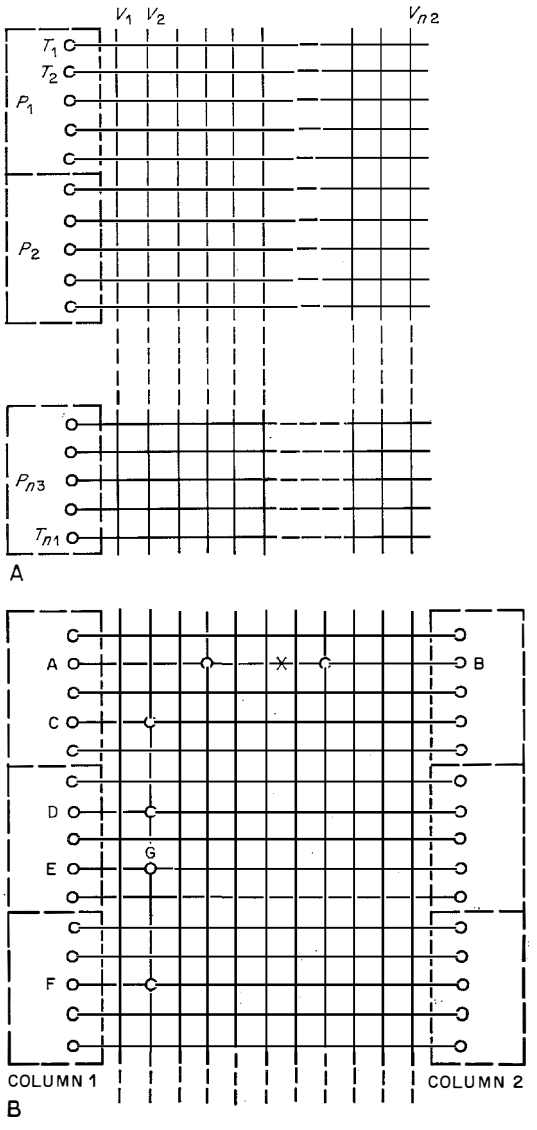

Figure 4—A 2-plane system of connections can be arranged in a matrix form which can theoretically accommodate any desired set of interconnections between a number of terminals.

The area required for wiring can be further reduced by arranging the components or circuit packages in two columns as shown in Figure 4*B* and sharing horizontal tracks between terminals in the two columns. On a chance basis there is a 1-in-2 chance that the connections from terminals *A* and *B* will be of the form shown, which is possible on one track broken at *X*, and a 1-in-2 chance that they will need to cross over, which is not possible on one track.

Logic circuits can normally be arranged to employ tracks on a better basis than chance since, for example, all the diode inputs to a diode gate are electrically identical. Thus the allocation of tracks can be interchanged to increase double use of horizontal tracks well above the chance figure.

In practice, vertical tracks can also be used more than once, since short connections (for example *C–D* and *E–F*) can share the same track provided a break is made at *G*.

Figure 5 shows a practical application of these principles to an *ISEP* plug-in unit [1]. Semiconductor integrated circuits in 8-lead *TO5* cans are mounted on a double-sided printed-circuit card. The integrated-circuit terminals are connected to a set of parallel tracks on 0·05-inch (1·3-millimetre) pitch on one side of the card. These tracks correspond to the horizontal tracks of Figure 4*B*. A set of tracks on the other side of the card, corresponding to the vertical tracks of Figure 4*B*, are through-connected to the first set to make up the required circuit pattern.

Figure 6 shows an extension of the principles which makes an even more efficient use of tracks for interconnecting 10-lead thin-film integrated circuits on a card. The extra efficiency is obtained by connecting each package terminal to a short vertical track which can be used to translate its position (by a through-connection) to any 1 of 10 horizontal tracks.

The main interconnection system consists of tracks running between the short translating tracks and leading to the connector.

These two examples illustrate how basic principles can be applied to produce practical arrangements which simplify both design and fabrication. The maximum use can be made of mass production since, for a wide range of application, cards with the same artwork are used. The difference between one circuit configuration and another is produced by making the appropriate through-connections and breaks. Apart from direct cost reduction, this reduces cycle times in both prototype and full-scale manufacturing stages. In the design stage, the highly rationalized arrangement reduces the amount of work either with manual or computer methods.

2.3 Multi-Layer Interconnections

The more layers that are used, the more complex is the interconnection pattern that can be accommodated in a given area. The cost of a multi-layer printed circuit, however, rises rapidly above 2 layers. Costs of inspection and the difficulty of changing or repairing inner layers must also be taken into account.

For these reasons application of multi-layer printed circuits is at present confined to cases where extreme compression is essential.

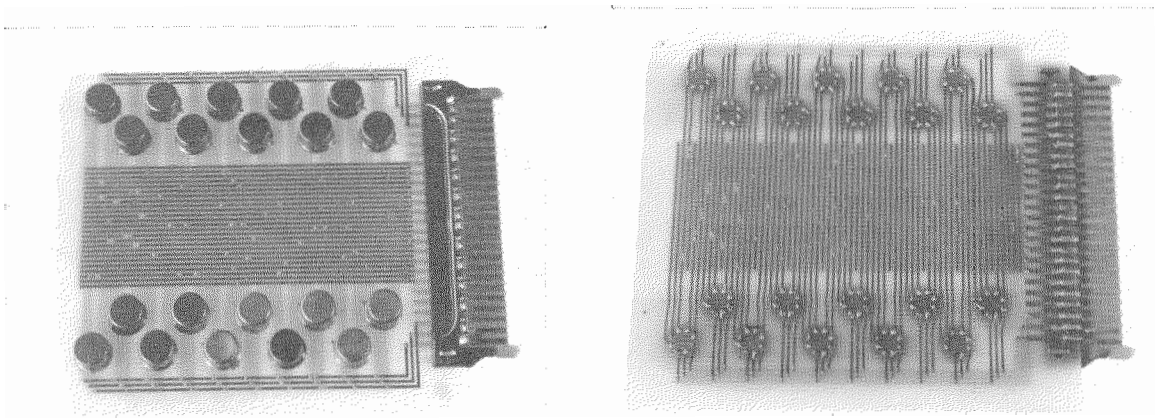

Figure 5—Top and bottom views of card approximately 4 inches (10·2 centimetres) square mounting 20 semiconductor integrated circuits interconnected by a 2-plane matrix.

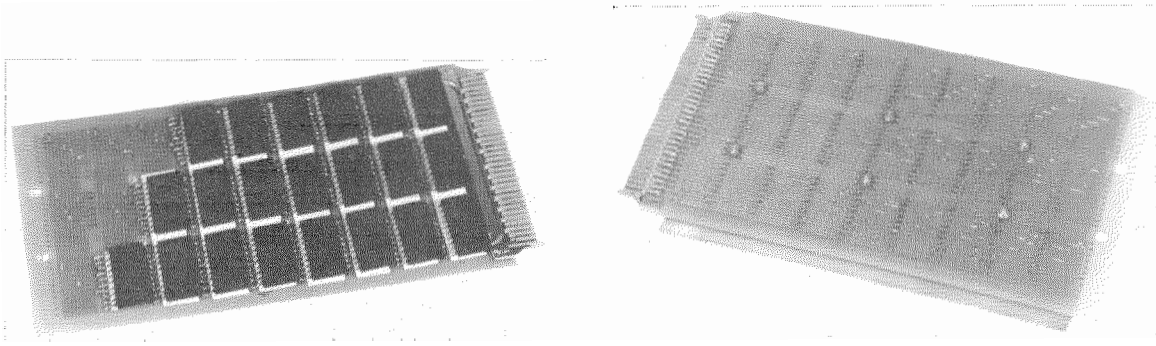

Figure 6—Interconnection of thin-film integrated circuits by a matrix with refinements to increase the efficiency of utilization of tracks. Both sides of the card are shown.

An important special case which might be considered a 3-layer system is the use of a third layer as an earth plane in high-frequency or high-speed equipment. Such an earth plane need not be continuous and a standardized perforated earth plane in the interior of a laminated board permits through-connection from surface to surface at the perforations.

2.4 Interconnection of Plug-In Units

The interconnection of a number of plug-in units (back wiring) can be achieved with only one or two layers in rather elementary cases. This problem will become more severe with the tighter packing of the future.

It is possible to rationalize wiring of this type in the following way. Figure 7 shows a typical field of terminals at the back of a subrack. The columns C_1 through C_{n1} each correspond to 1 plug-in unit. The wires connected to terminals in such a field may come from external points and then connect to other terminals in the field; on the other hand, the wires may merely interconnect the terminals. Considering the interconnections between terminals in the field, we have the following:—

(A) Since each column corresponds to 1 plug-in unit, there is no requirement for wires connecting 2 terminals in the same column.

(B) Consider now a wire connecting a terminal in any one column, say C_1, to a terminal in any other column, say C_r. If the pin in column C_1 is in row s, then—provided there is freedom of terminal layout on the plug-in unit—the pin in column C_r can also be in row s.

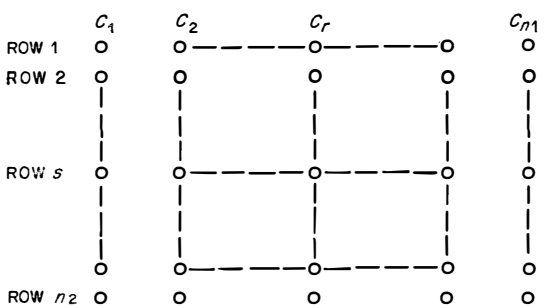

Figure 7—Diagram of the field of terminals at the back of a subrack. It is possible to arrange for the majority of the wiring to run horizontally.

From **(A)** and **(B)** it follows that all the interconnections between terminals in the field can be in the form of straight wires running horizontally across the field. In the case of a connection coming from an external point it is obvious that the same arrangement can be used. The minimum number of wires running along any row is 1, for example, earth or high-tension. The maximum number for n columns is n. For example, in carrier telephone channelling equipment each audio input comes from a separate external point.

This argument assumes complete freedom of terminal layout on every card. The practicability of this depends on the sensitivity of the interconnection system used on the card to this constraint. The matrix arrangements described in Section 2.2 are able to meet this requirement, since the appropriate allocation of tracks can be made the starting point of card design. There are also good facilities for translating connections from one track position to another by through-connection to tracks on the other side of the card.

However, even if there is no technical difficulty in complete rationalization of back wiring in this way, there may be other difficulties. For example, it may be desirable for manufacturing and maintenance reasons to use the same type of plug-in unit in various parts of the equipment. In general, the terminal allocations required will be different in the various card positions.

This difficulty can to some extent be overcome by the use of redundant terminals. In practice, it is unreasonable to attempt to put all wiring into the rationalized form. It does appear possible, however, to deal with the majority of the wiring in this way.

There are several advantages of arranging back wiring in this way. Manufacture is simplified and automation facilitated, whether ordinary

wire or materials such as flexible printed circuits are used. In simple cases an ordinary single- or double-sided printed-circuit board, possibly supplemented by some other wiring, may suffice. Because of the simple arrangement, more wiring can be packed into a given space. Design and preparation of manufacturing information are simplified.

This type of interconnection system can be applied only if there is sufficient room between terminals in a column to accommodate at least one thickness of wire or flexible printed circuit. Several conductors can then pass along one row, one above the other. Since the spacing of columns (that is to say, cards) is normally greater than the spacing of terminals in a column, it follows that, to obtain increased terminal density in the future, it is better to increase the number of columns of terminals corresponding to a card rather than to decrease the vertical terminal spacing to the point where simple horizontal wiring is difficult or impossible.

3. Future Trends

The technology of integrated circuits, mounting and interconnection techniques, and new circuit concepts are all developing rapidly. While it is clear that significant size and cost advantages are theoretically possible, many problems must be overcome before these advantages can be realized in practice. Some of the advantages of integrated circuits are already being realized using existing assembly techniques such as printed-circuit cards, and the adoption of more-sophisticated techniques will be evolutionary.

A key factor in the application of the new techniques will be the development of sound manufacturing methods for packaging and interconnection that are compatible with the size and cost advantages expected by the use of integrated circuits. This means the introduction of more-complex machinery into the assembly factories and the greatly increased use of automation for the handling of small parts, if low costs are to be realized. The further development of fundamentally simple rationalized interconnection schemes will facilitate standardization and the automation of manufacturing and design.

The decreasing cost of integrated circuits and the increasing complexity of the circuits attainable on one chip should lead to a reduction in the use of bulky components such as inductors. Considerable effort is being applied to develop circuit techniques for replacing passive networks by active networks without inductors, and to develop entirely digital systems as alternatives to linear systems. Therefore, a greater uniformity of techniques is to be expected in the future between types of equipment which at present differ radically.

Increased reliability should lead to a decreased use of plugged connections and greater use of semi-permanent or permanent connections, thus further reducing costs and increasing reliability.

4. Acknowledgments

The authors wish to acknowledge the contributions made by their colleagues in the companies of ITT Europe to the work described in this paper.

5. References

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Mr. Prior is an Associate Member of the Institution of Electrical Engineers.

Projektierungsunterlagen für Vermittlungssysteme (Teletraffic Engineering Manual)

This manual contains all traffic data needed for the design of switching systems produced by Standard Elektrik Lorenz. The traffic tables and diagrams can be used also for other—even future—switching systems, assuming the same theoretical treatment of traffic.

The manual is divided into the following chapters:

1. Switching Network Terms
2. Telephone Traffic Terms
3. Loss Formulas for Single-Stage Arrays
4. Dimensioning of Single-Stage Arrays
5. Dimensioning of First-Choice Trunk Groups
6. Dimensioning of Line-Finder Arrays in the *HKS* System
7. Dimensioning of Line-Finder Arrays in the Large-Size Crossbar System
8. Dimensioning of Waiting Systems for Exponentially Distributed Holding Times
9. Dimensioning of Waiting Systems for Constant Holding Times
10. Sampling and Scanning Errors of Traffic Measurements

The definitions in the first three chapters and the explanatory introductions to the following table and diagram sections facilitate use of the manual. In addition, the manual contains a large number of examples showing possible applications.

The book of 453 pages is published by Standard Elektrik Lorenz, 42 Hellmuth-Hirth-Strasse, 7000 Stuttgart-Zuffenhausen, Federal Republic of Germany. It measures 11 by 15 centimeters (4.4 by 5.9 inches) and sells for DM 4.

Improving Performance and Functional Flexibility of Thin-Film and Semiconductor Integrated Circuits

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1. Introduction

Integrated circuits, such as thin-film and semiconductor, are already proving their advantage over lumped components by virtue of their low cost, high reliability, and small size. For most applications it is no longer necessary to make concessions in performance specification so that microcircuits can be used. Performance can, in fact, be superior to that obtained with lumped components, particularly where transmission delay through interconnecting leads becomes embarrassing. There is still one very prominent characteristic peculiar to microcircuits, namely, the severe handicap imposed on functional flexibility. This paper describes a new approach to fabrication techniques intended ultimately to remove restrictions on functional flexibility without impairing the advantages of microcircuits over lumped components.

The approach is to fabricate the substrate so that most of the processing is complete before it is committed to the desired circuit function. Until the last function-defining process, the substrate could be used for any function within the capabilities of the integrated circuit process. This basic philosophy can be applied quite generally to integrated circuits, but the techniques depend on the material and processes. The paper shows application to thin-film circuits and to semiconductor integrated circuits.

2. Need For Functional Flexibility

When integrated circuits were first launched, there was much controversy about the lack of functional flexibility. Semiconductor integrated circuits were criticized on the basis that it was not possible to optimize systems if the circuits were restricted to a standard range of digital blocks. However, it soon became obvious that circuit standardization could by itself bring economic advantages, and in the large market in the United States standard digital circuits became available at a cost which made them the most economic components. Hence, the problems associated with inflexibility receded, while designers either accepted standard circuits or used conventional components. More recently, several factors have emerged which make it worth while to tackle the problem of increasing the functional flexibility of microcircuits.

The first consideration concerns the use of standard circuits. Improved techniques for both thin films and thick films and, especially, improved performance in semiconductor integrated circuits make these devices attractive for many new applications besides digital circuits. However, standardization is much more difficult to apply to non-digital circuits, and unless a particular circuit is manufactured in large quantities, production costs per device are high. This explains the superiority of thin-film techniques for analogue applications for, in the foreseeable future, it must remain a luxury to use conventional semiconductor integrated circuits with their inherent high tooling costs for non-standard applications.

Even in the digital field standardization can cause problems. Local conditions in smaller countries sometimes make the universal standard unacceptable, although the quantities required of the acceptable device are so low that they do not justify the tooling costs. Perhaps the biggest restraint on standardization for digital applications comes from the recent trend of larger sub-systems. Yields and reliability of semiconductor integrated circuits are now so high that it becomes sensible to think in terms of very complex sub-systems comprising perhaps a single slice containing several thousand components. Clearly, as the complexity of the integrated circuit increases, so the widespread use of the standard integrated circuit becomes less likely. Where the electronics of a large system may be contained entirely on a few

slices, functional flexibility becomes essential if excessive tooling cost per slice is to be avoided.

The second consideration concerns production. There is a better chance of optimizing yields and performance where there is only one main product, rather than several smaller batches of different products each being identified by function from the first stages of manufacture. Thus, a technique for manufacturing universal substrates, where the function is defined at the end of the production sequence, enables the manufacturer to obtain a high volume throughput for a single product, even if his orders are for circuits covering a wide variety of functions. As microcircuits are being applied to a wider field, the question of distribution of contributed value becomes more important. Much of the contributed value of a sophisticated electronic system comes from the design and testing of the circuits. The component manufacturer may not have such skills and plant nor may he find it worth while to invest extensively in them. The systems manufacturer, on the other hand, may need the contributed value from design and test to maintain his profit level and justify his existence. The flexible approach would allow the system manufacturer to purchase the universal substrate, carry out his own design, function-defining process test, and mounting. This gives a more convenient distribution of contributed value, and leaves the component manufacturer free to optimize the large-scale production of universal substrates.

Finally, the greatest impetus to a universal-substrate approach may stem from progress in automation of the design of electronic systems. It is now becoming feasible that a slice subsystem of the type previously mentioned can be based on a computer design. It seems a pity that a design in digital form must then be converted into a circuit layout drawing, a microcircuit design, and finally a photographic mask then used to control the production processes. With a universal substrate it should be possible to programme the final function-defining process directly with the digital output from the computer.

3. Functional Flexibility in Thin-Film and Semiconductor Integrated Circuits

Integrated circuits such as thin-film, thick-film, monolithic semiconductor, et cetera, may be described quite generally but precisely in terms of the physical properties and dimensions of a laminar substrate. Let the coordinates in the plane of the substrate be $x,y,$ and let z be the direction perpendicular to the substrate (see Figure 1). Let P denote the physical properties at any point in the substrate, with $P(z)$ being the function of P in that direction with x and y fixed, and $P(xy)$ being the function of P in a plane defined by a fixed value of z.

The present-day integrated circuits are manufactured by a series of alternate $P(z)$ (materials) and $P(xy)$ (function-defining) processes. The circuit function is "frozen in" at the earliest stage of manufacture because the masking processes are essentially two-dimensional and an area-defining step must usually be carried out before the next $P(z)$ process. If these processes could be separated, so that most of the $P(z)$ steps could be carried out before the $P(xy)$ stages, substrates could be manufactured and stored for subsequent final conversion into functional circuits.

In theory, the simplest way of separating the $P(xy)$ process from the $P(z)$ process is to use

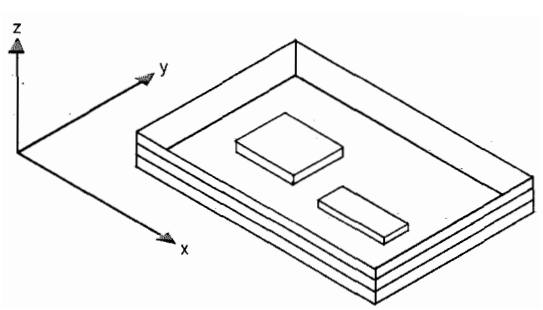


Figure 1—General representation of an integrated circuit.

a 3-dimensional process for defining the function. This is analogous to the selective activation of the emulsions in a multilayer colour film by the red, green, and blue components of the image. In practice, selective activation of layers in integrated circuits presents some formidable technological problems. However, for most purposes, it is not necessary for the upper layers to remain in situ while the lower layers are processed. Thus it has been possible to use substrates which have all the layer deposition processes complete, and then remove selectively and shape the individual layers to give the desired circuit function. For thin-film circuits this may be carried out by selective etching. For semiconductor integrated circuits it is much more difficult to apply selective etching. Devices have been made using multilayer epitaxial silicon substrates and shaping these layers after deposition by a precision spark erosion process. This also puts severe demands on the technology, since the control in the z direction must be within a fraction of a micron. For substrates capable of producing high-speed active devices, the tolerance on z is of the same order as the positional control and the work damage of the process at the present state of the art.

There is another way of separating the $P(xy)$ processes from the $P(z)$ processes which is more compatible with present-day technology. In this method, the substrate is divided into "cells" which for access terminate entirely in a single xy surface plane so that the function can be determined by a single, final, 2-dimensional $P(xy)$ process [1]. The cellular approach is analogous to the shadow-mask method of reproducing a colour picture on a cathode-ray tube. In this case, a screen is divided into cells, each containing an area of red, green, and blue phosphor, and depending on the colour required, the appropriate combination of phosphors is activated by the electron beam. Each group of red, green, and blue phosphors represents a cell, and the system relies on the smallest area to be clearly resolved being several times the size of one cell. An integrated circuit can likewise be divided into minute cells, each cell containing every one of the layers which might be called into play to perform a particular function. If the access to all the layers of each cell is now made from one face, then the function-defining process again becomes a 2-dimensional one. Universal substrates based on thin-film technology and cellular semiconductor integrated-circuit technology are discussed in Sections 5 and 6 respectively.

Both the 3-dimensional and the cellular approach discussed so far have implied the use of precision photographic masks at some stage of manufacture. The key to functional flexibility is to isolate the function-defining $P(xy)$ process from the processes that go into the drawing and preparation of the photographic mask. This has been achieved with the microengraving process, which can be used directly on the integrated circuit to perform the precise function-defining $P(xy)$ process. It can be used either in conjunction with a coarse 3-dimensional process or directly on the universal substrate. Further, this type of process is ideally suited to computer control so that the direct transition from design automation to device pattern is facilitated.

In the next two sections, a technique for improving the flexibility of thin-film circuits is described in detail, while in Section 6 an approach to the problem of flexibility in semiconductor integrated circuits is outlined.

4. Fabrication of Microcircuits Using Microengraving

4.1 Microengraving

Microengraving can be used for both thin-film and semiconductor integrated circuits, but its particular applicability to flexible thin-film-circuit fabrication is mainly dealt with in this section.

The primary requirement in the introduction of automatic digital control to the fabrication of microelectronic circuits is for a process capable

of precise machining of deposited thin films. One solution is to use the thermal effects of focused electron or laser beams, and much work is at present being done along these lines. Such processes are as yet experimental, and the overall complexity of the systems involved, particularly in the case of the electron beam, makes it unlikely that suitable equipment will be available in the near future for economic manufacture of microelectronic circuits.

A simple method of machining thin films, using spark discharges, has been developed in which the accuracy, resolution, and machining speed are adequate for many of the applications involved in the fabrication of thin-film and semiconductor integrated circuits.

4.2 Principles of Operation

The technique of microengraving evolved from a study of the micromachining of bulk materials using spark discharges.

Spark machining is well established as a method of machining electrically conductive materials by the erosive action of spark discharges in a dielectric medium. The sparks occur between the work material and a tool electrode which progresses into the work automatically by servo control to reproduce the electrode shape precisely in the work piece.

It is not intended in this paper to give details of the spark erosion process as such, but it is important to note some of the relevant points arising out of this work.

The main factor controlling the ultimate resolution attainable in spark-discharge machining is the energy dissipated in the spark, which governs the spark-crater dimensions. Electron micrographs of eroded surfaces showed that a large ratio exists, about 20:1, between the diameter and depth of a sparked crater. In the machining of bulk materials (for example, apertures in a metal plate), it is the crater depth that determines the edge definition obtained, once the eroding electrode has penetrated below the surface of the plate. In micromachining applications, useful work can be done with an edge definition down to about one micron; below this value, the rate of erosion becomes too low for practical use.

For engraving thin conducting films on insulating substrate, the penetration required is often less than 100 angstrom units, and rarely greater than a few thousand angstroms. The possibility arises of cutting lines, using a single point electrode moving over and close to the film surface, each spark removing a small area of the film. In this case, however, the resolution obtained is determined by the spark-crater diameter, and considerable reduction in input energy is called for. The use of low voltage to achieve this introduces problems of maintaining minute spark gaps of a few microns only, and traversing the surface area demands a degree of flatness and parallelism that is difficult to achieve in practice.

The use of an engraving probe or stylus, traversed whilst in contact with the film surface, tends to erode the surrounding area, and some progress can be made in this way on extremely thin films. The process, however, is completely unreliable because of the tendency to short-circuit the stylus to the film surface, which stops further erosion. On films where the thickness is greater than the crater depth, a continuous short-circuit occurs.

The solution adopted is to vibrate the stylus perpendicular to the plane of the surface being engraved, so as to make and break contact to the film and produce momentarily the critical gap conditions for spark breakdown during each half-cycle of movement.

The spark energy is provided by a small capacitor placed across the gap and charged through a resistance from a low-voltage direct-current supply. The value of the charging resistor must be sufficiently large to prevent thermal damage to the film due to flow of direct current. The optimum voltage and component values are dependent on type and thickness of the material being engraved; typical values for nichrome

films less than 100 angstroms thick are: 24 volts, 50×10^{-12} farad, and 10^5 ohms. The process is carried out under the surface of a dielectric fluid which provides high breakdown strength and restricts the breakdown to an area closely defined by the stylus diameter.

4.3 Engraving Head

The essential requirement of the head assembly is that it should maintain the stylus in light contact with the surface to be engraved and accommodate the maximum degree of unevenness likely to be encountered at the substrate. Freedom of movement must be restricted to the absolute minimum in all directions except in the vertical plane. This is accomplished in the design illustrated in Figure 2, which consists of three main parts: a balanced arm, a transducer element, and the engraving stylus.

The balanced arm is supported by two steel strips extended on either side of the arm. The exposed length of the strips is such that they bend freely in their thickness, but lateral movement of the arm is restricted. Means are provided for adjusting the balance of the arm to obtain the correct pressure on the film surface.

The transducer is a piezoelectric element which is caused to vibrate in a longitudinally bending mode by the application of a driving voltage to metallized electrode areas. When energized in a resonant mode, for example at 4·5 kilohertz, a tip movement of approximately 25 microns is obtained with 100 volts input. One end of the transducer is rigidly clamped to the balanced arm, and the stylus is mounted at the free end.

Several conflicting factors arise in the design of the stylus and its mounting. The tip diameter must be precisely controlled, and close tolerances maintained in use, independent of wear. Any lateral movement of the tip affects positional accuracy and the edge definition of the engraved line. Some resilience must be introduced into the stylus mounting to avoid deformation of the tip by continuous hammering action. These conditions are found to be met in the design shown in the inset to Figure 2,

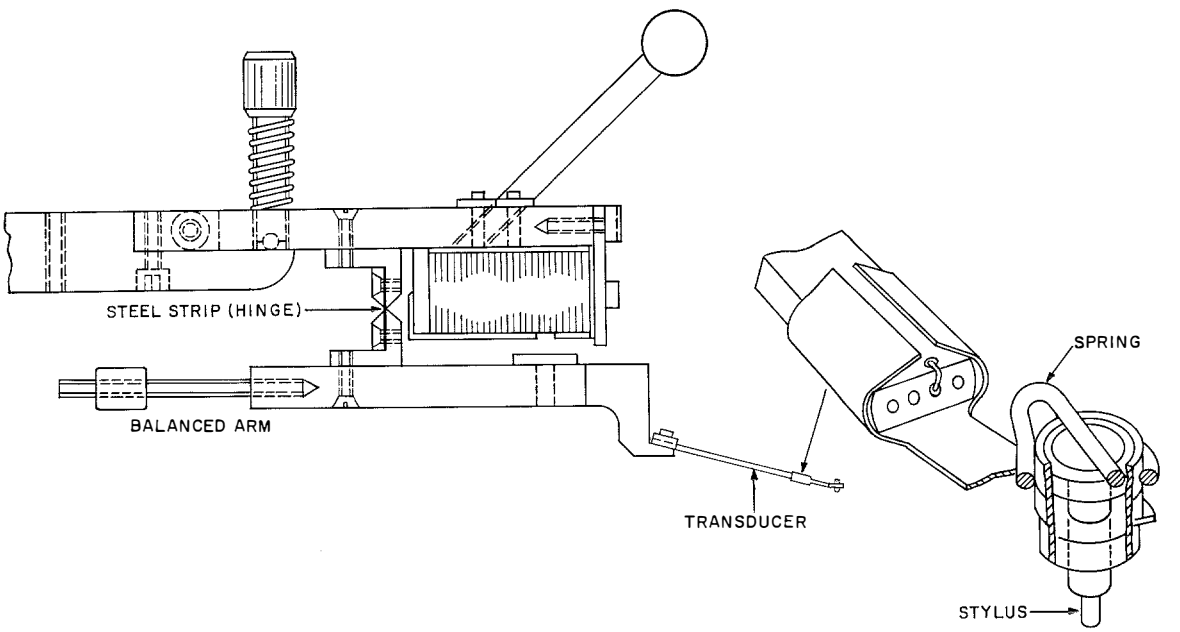


Figure 2—Engraving head.

which is based on component parts manufactured cheaply by the watch industry. The stylus is housed in jewelled bearings; a 1-micron radial clearance is found to be adequate to provide free longitudinal movement. A spring wire ensures correct seating of the stylus and provides the required degree of resilience. The stylus is easily replaceable.

4.4 Operating Characteristics

The capabilities of the technique have been assessed for specific thin-film engraving applications; nichrome resistance films [2], gold and aluminium films for conductors, and specially prepared hard metallic coatings for the preparation of in-contact photoetching masks.

The mechanism by which material is eroded is well illustrated in Figure 3. This photograph shows a portion of a track 50 microns wide engraved in a nichrome film 70 angstroms thick. The surface is seen to consist of a series of craters, each approximately 5 microns in diameter. Any residual material between the craters is electrically isolated, and the measured leakage current across a track 1 centimetre long is less than 10^{-12} ampere with 25 volts applied. The eroded material condenses in the dielectric and settles on the substrate. This must subsequently be removed by ultrasonic cleaning.

The engraving speed which can be used depends on the volume of material to be removed. Typical values for a 50-micron-wide track are: 1 centimetre per second for nichrome 70 angstroms thick, and 1 millimetre per second for gold film 3000 angstroms thick.

Fine control of engraved track width can be obtained by varying the applied voltage, but as this is primarily set for the required edge definition, the track width is normally determined by the stylus diameter. The range of track widths obtainable in a single pass lies between 10 and 250 microns. For track widths greater than 50 microns, the stylus is made with a parallel-sided tip, so that a constant diameter is maintained as the length of the parallel portion is eroded away during use. A 50-micron-diameter stylus engraves a line length of approximately 1 metre per micron of wear, which gives a minimum of 250 metres of engraved track per stylus. A tapered stylus is used for engraving track widths less than 50 microns, and in this case electrode wear becomes a limitation where close tolerances on track width have to be maintained.

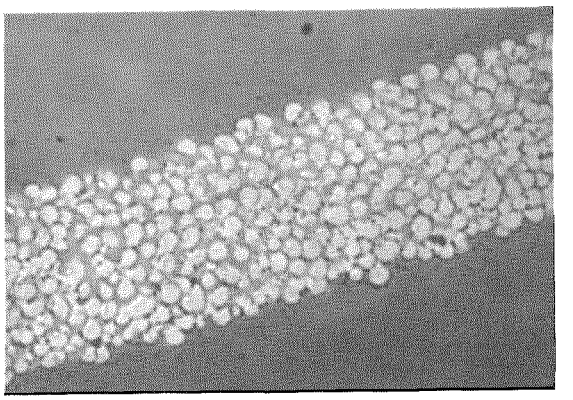


Figure 3—Section of microengraved track 50 microns wide.

Large areas can be blocked out by scanning the film surface at a pitch smaller than the stylus diameter.

4.5 Tape-Controlled Operation

The engraving head has been adapted for automatic working by incorporation into a tape-controlled pattern generator. This was designed and built specifically for this purpose, and the complete equipment is shown in Figure 4. The coordinate stage is driven by stepping motors and has a positional accuracy of ± 6 microns over 5 centimetres of travel. Information is fed in on standard telex tape and contains details in X and Y coordinates of all positional change points, plus instructions regarding speed and engraving conditions. Electronic control is effected by comparison of two registers. The information on table position is compared with new information received from

the tape, and the table moves until the information corresponds in the two registers.

The capabilities of the equipment are illustrated by the simple pattern reproduced in Figure 5. The track width in the central grid section is 25 microns with variable spacing down to 10 microns. The lines enclosing the square are 65 microns wide, and the blocked-out areas are made with 65-micron lines at 30-micron pitch. The actual size of the pattern is 3·1 millimetres square.

At the present stage of development, the combined accuracy of the engraving head and coordinate stage is ±10 microns. This enables 250-micron-wide resistor stripes to be directly engraved to ±5-per-cent tolerance. Much closer tolerance is maintained on multistripe or meander resistors due to cancelling of errors.

5. Application to Manufacture of Thin-Film Circuits

There are several ways in which microengraving can be applied to improve the performance and functional flexibility of thin-film circuits. It may be used to adjust the passive components after completion of deposition processes so that special or close-tolerance values are obtained. It can be used for direct engraving of precision masks for in-contact photolithography, and also for direct delineation of resistor patterns. As such, it can have application ranging from small-scale modelling to large-scale manufacturing using digital control.

5.1 Value Adjustment of Thin-Film Components

It is often necessary, particularly in linear circuits, to obtain components to very close tolerances. It also happens, in the manufacture of a wide range of thin-film circuits, that the yield is often affected by a single out-of-tolerance component.

The suitability of microengraving for adjustment of thin-film resistors and capacitors has been established, and adjustment to better than 0·1 per cent is readily achieved. It is a useful feature of the technique that the engraving voltage can be suitably adjusted to cut only the top plate of a thin-film capacitor. This permits the adjustment of capacitors without degrading the performance by formation of short breakdown paths. Resistor values can be continuously monitored during adjustment, but the process

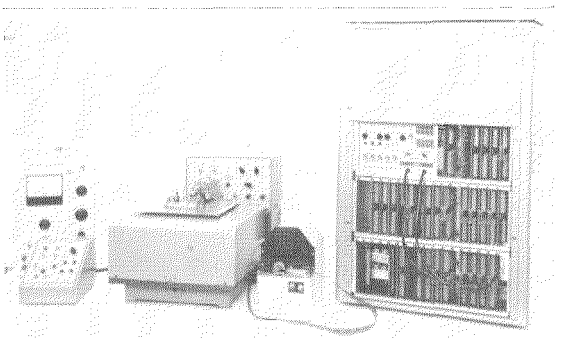


Figure 4—Complete autoengraving equipment.

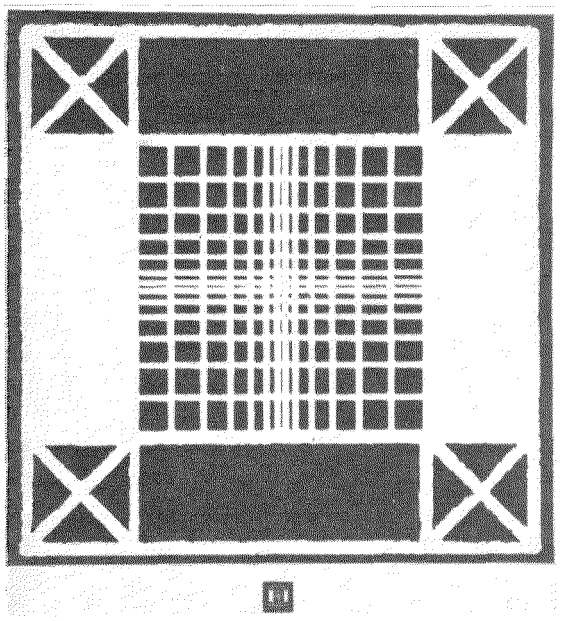


Figure 5—Microengraved test pattern. Actual size is 3·1 millimetres square.

has to be interrupted for measurement of capacitance. Using a hand-operated machine with adjustable contact probes, the time taken for setting up a substrate and adjusting a resistor to within to 0·1 per cent of selected value is 1 minute; the corresponding time for a capacitor is 3 minutes. Further reduction in time could be effected by automatic working.

It is often advantageous to carry out operational adjustment rather than adjust individual components. For instance, the frequency of an inductance-capacitance circuit can be set by adjusting the capacitance after the inductance has been inserted.

Extensive life tests have been carried out on adjusted resistors and capacitors, which had standard components on the same substrate. The results obtained show no difference between the microengraved and standard components.

5.2 Combination of 2-Dimensional Process with Microengraving

This process is based on the use of a standard substrate with superimposed layers of resistance and conductance material. Recent advances in selective etching processes for gold and nichrome provide improved substrates with closely controlled sheet resistivity. The microengraver can be programmed to produce a photo mask directly to size for defining the interconnection pattern. Chemical etching of the gold layer exposes the underlying resistance film which can be directly microengraved to form the required resistor pattern. Surplus nichrome film is isolated in the process and need not be completely removed. Where close-tolerance resistors are required, resistors can be adjusted at the same time as defining the area.

The stages involved in this process are illustrated in Figure 6. The desired circuit configuration (Figure 6*A*) is first laid out on squared paper, and two taped programmes are constituted from the positional change points. The first tape is used to engrave a mask (Figure 6*B*) for etching the interconnection pattern (Figure 6*C*), and the second programme controls the engraving of the resistor areas and isolated lands for transistor mounting (Figure 6*D*). The engraving time for the master mask, done at low speed, is 12 minutes, and the total engraving time for each circuit is 27 seconds.

The system can be used for decentralized manufacture at minimal plant investment or alternatively decentralized design and programming telexed direct to a manufacturing centre. The

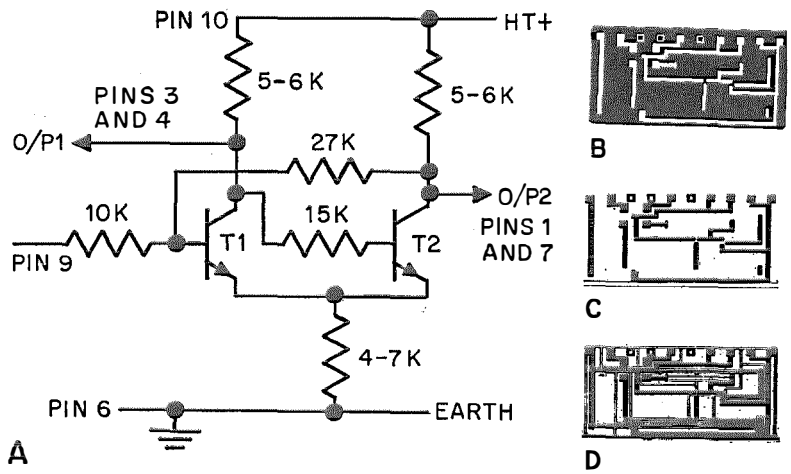


Figure 6—Four stages in producing the microengraved circuit at *D*. *A* is the circuit diagram, *B* is the microengraved photographic mask, and *C* is the etched interconnection pattern.

system can be extended to include capacitors by allocating parts of the substrate for this purpose during the initial manufacture of the substrate. A single capacitive area would suffice, as this can be cut up into individual capacitors by microengraving.

5.3 Standard-Pattern Universal Substrate

This is an alternative system useful for modelling and small-scale manufacture of thin-film circuits where microengraving need be the only additional process involved in converting a standard pattern into the required circuit configuration.

The standard-pattern substrate consists essentially of an "all-over" resistive film with a superimposed conductor pattern. The films may be of nichrome and gold-chrome respectively. One proposal is based on a substrate consisting of rectangular islands of nichrome surrounded by a continuous grid pattern of conductor. The microengraver is programmed to delineate the required resistor; interconnection pattern and active components are inserted where necessary. A second proposal suggests isolated conductor lands distributed over a resistance area. These lands serve for terminating microengraved resistors, and for attaching links and leads of added components. The second proposal has an advantage in that only nichrome needs to be engraved, which can be done at high speed. The total engraving time for a typical thin-film circuit on a substrate 1 inch by 0·5 inch is 35 seconds and 7 seconds respectively. Both systems are capable of being extended to integrated resistance-capacitance networks.

The use of standard patterns detracts somewhat from the complete flexibility offered by the system described in Section 5.1, but a selected range of standard-pattern substrates would meet the demands of a wide variety of circuits.

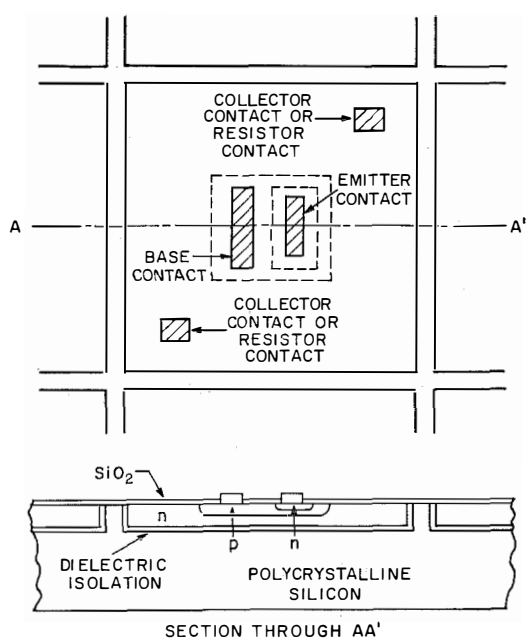


Figure 7—Example of cell for cellular substrate.

6. Cellular Semiconductor Integrated-Circuit Techniques

6.1 Example of Cellular Circuit Design

The problems involved in increasing the functional flexibility of semiconductor integrated circuits are quite different from those encountered in thin films, and for the reasons given in Section 3 a cellular approach seems to be the most promising.

The basic objective of the cellular approach is to produce an array of identical cells from which circuit functions can be built up. Figure 7 shows a type of cell suitable for this purpose. This is basically a dielectric-isolated planar transistor structure with two collector contacts. It would be as small as technology permits and can be connected in various ways to form different components or parts of components. Transistors of any desired power-handling capacity can be made by paralleling the appropriate number of cells: diodes by using the emitter or collector junctions, resistors by using the collector-collector bulk resistances in series-

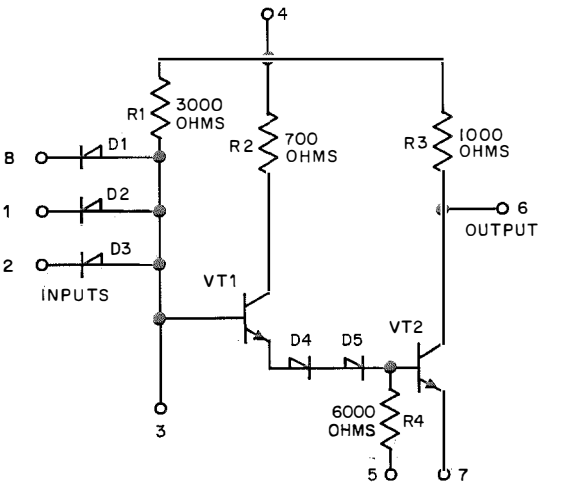
parallel combinations, and capacitors by paralleling sufficient reverse-biased collector junctions. By laying down the appropriate interconnection pattern, any circuit can, in principle, be synthesized. As an example, let us consider a simple diode-transistor-logic gate circuit (Figure 8). If we take a cell with a collector-collector resistance of 400 ohms, the required cellular array could be as in Figure 9, where, for illustrative purposes, 4 cells have been wired in parallel for each transistor. Several points are evident from this layout.

(A) The cells can be interconnected to avoid crossovers.

(B) There need be no unused cells inside the overall outline.

(C) Most of the area is used for resistors, whereas diodes and transistors (even if composed of a generous number of cells connected

Figure 8—Diode-transistor-logic circuit.



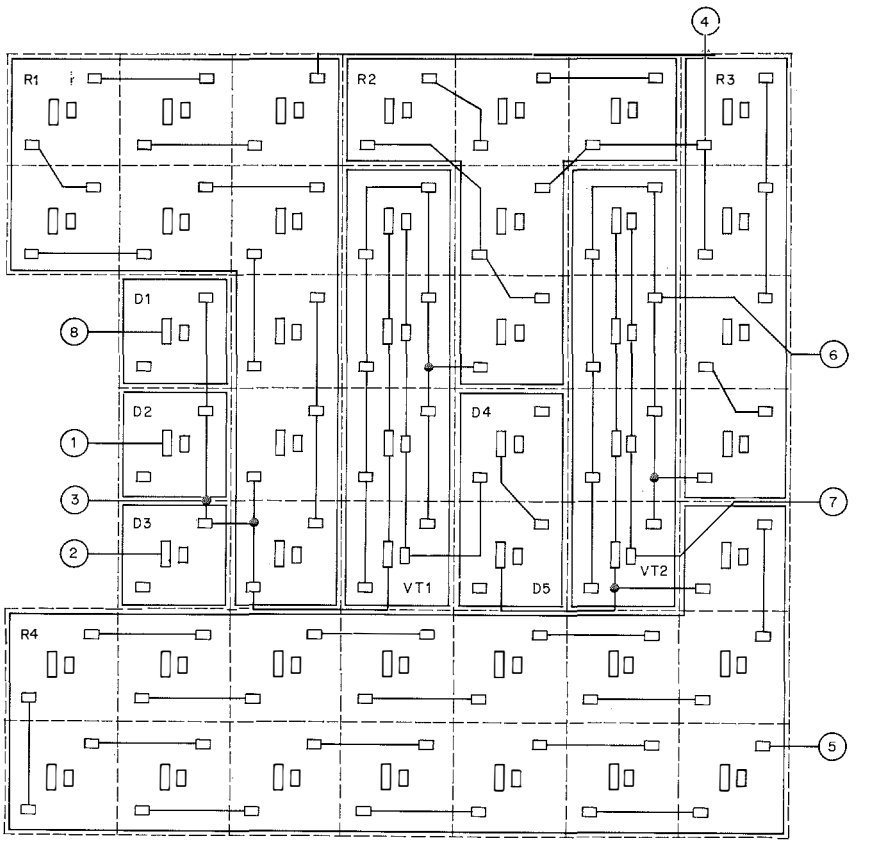


Figure 9—Circuit of Figure 8 formed on a cellular substrate with 400-ohm cells.

in parallel) use little area. Thus, in common with conventional integrated circuits, the cellular approach is more efficient for circuits having mostly diodes and transistors and relatively few resistors. Initial work on cellular circuit design indicates that the optimum cell resistance would be about 1000 ohms. This is difficult to achieve with the cell shown in Figure 7, and it should be borne in mind that a high collector-collector resistance brings with it the penalty of a high saturation resistance if the cell is used as a transistor, even though this is minimized by connecting the two collector contacts together. To avoid these difficulties, a new type of cell is being designed which incorporates the resistor function into the base diffusion, enabling cell resistances of 1000 ohms to be obtained easily while still allowing low-saturation-resistance epitaxial transistors to be realized by the same cell.

6.2 Computers for Design and Fabrication

As electronic equipment becomes more complex, the task of designing microcircuit layouts and processing masks becomes increasingly laborious, and computer techniques for performing most of this work would be very valuable. The regular character of the cellular substrate for semiconductor integrated circuits makes it particularly amenable to computer-controlled processing. Techniques for designing circuit layouts by computer are still in the development stage, but much tedious work can be eliminated even with present techniques. For instance, the interconnection mask can be made by converting the cellular layout into digital information which can be fed direct to the tape-controlled microengraving machine. Platinum film fired onto borosilicate glass makes a suitable mask material. These opaque films have good abrasion resistance and can be made very thin, so that fine lines with edge definition adequate for present purposes can be obtained. As tolerances on semiconductor substrates become tighter, the possibility of engraving a scaled-up mask and reducing it photographically might be considered. An alternative way of fabricating interconnection masks as cell sizes decrease would be to use a laser combined with a tape-controlled table. Although there is much scope for further work, we have already machined 5-micron-wide lines, which should be narrow enough at least for the immediate future. Figure 10 shows an interconnection mask microengraved for the layout shown in Figure 9. The cell pitch here is 0·69 millimetre, a figure chosen to facilitate initial experiments; much smaller cells would however present no fundamental problems.

Other interesting advantages stem from the sub-component nature of the cells. Redundancy, if desired, can be incorporated at component level rather than at circuit-function level. Also, if a convenient method of cell-by-cell testing can be developed (for example, using a scanning electron beam [3]) the design computer

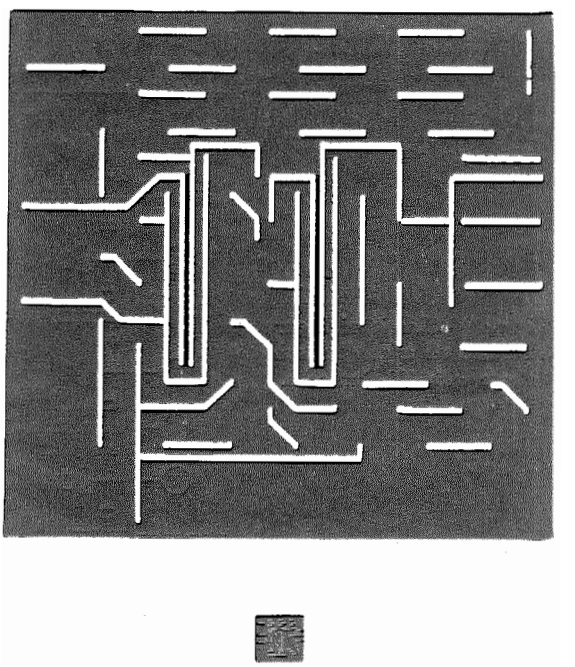


Figure 10—Interconnection mask for circuit shown in Figures 8 and 9. It is cut by a tape-controlled microengraving machine.

could be supplied with the test record, so that defective cells are not incorporated. This would improve the overall yield, and would be particularly valuable when it is attempted to put a very large number of circuit functions on a single slice.

6.3 Isolation Techniques

The commercial prospects of the cellular substrate depend on a cheap and reliable isolation technique which does not waste too much slice area. As other techniques needed for cellular substrate fabrication (photolithography, diffusion, et cetera) are relatively well developed, initial experimental work has been largely on isolation.

6.3.1 *Conventional Dielectric Isolation*

Dielectric isolation, which is preferable to diffused isolation, can be obtained by a "trenching and backfilling" process [4]. However, it is difficult to cut reasonably deep troughs narrow enough to avoid wasting area. Shallow troughs, of course, make the reverse lapping critical and expensive. An effective method of spark eroding grids has been developed using a special type of louvred electrode with blades 25 microns thick. Grids down to 0·25-millimetre pitch have been eroded 0·1-millimetre deep in silicon. Smaller pitches can be obtained, but the proportion of slice area wasted in the troughs becomes prohibitive.

6.3.2 *Novel Isolation Techniques*

Another technique has been developed which is particularly applicable to cellular substrates. The process, shown in Figure 11, is as follows.

(A) A single-crystal silicon slice is lapped and polished to give accurately flat and parallel faces.

(B) A 1-micron layer of silicon nitride is deposited on one side.

(C) A thick layer (say 200 microns) of polycrystalline silicon is deposited on the nitride.

(D) The single-crystal layer is air abraded to reduce its thickness to 12 microns or less.

(E) The slice is coated with photoresist and exposed through a mask of the desired isolation pattern.

(F) Isolation troughs are etched down to the nitride layer, which is very inert chemically, leaving isolated islands.

(G) The silicon surfaces are passivated with a thermally grown layer of silica.

Cells can then be diffused into the islands in the normal way. Due to the thinness of the single-crystal layer, very small land separations can be obtained, the definition being limited only by the photolithography. The troughs are so shallow that interconnections can be laid across them, but if desired, they can be filled after stage **(F)** by depositing a layer of silica at least as thick as the trough depth, and lapping down flush with the tops of the silicon

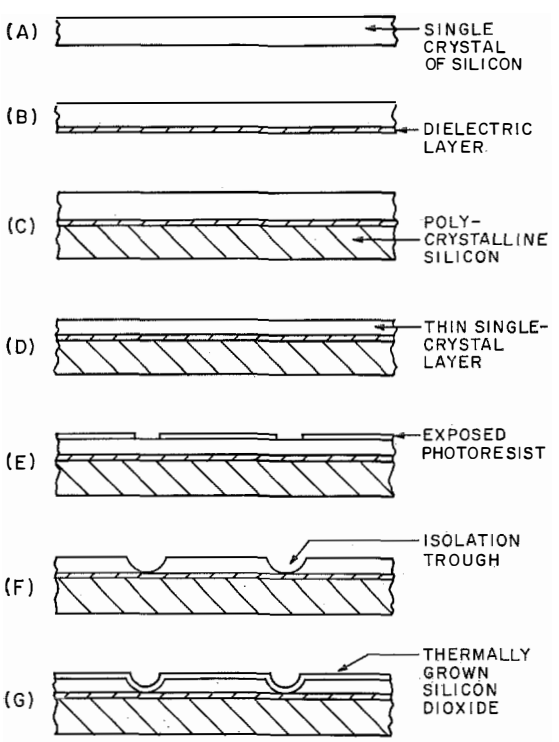


Figure 11—Isolation process in cellular substrate.

islands again. As relatively little material has to be removed, the lapping operation is quite straightforward.

The technique can also be applied to conventional integrated-circuit isolation. The procedure is the same down to stage **(D)**, but after this the devices are diffused and the interconnections laid down in the normal way. Isolation is provided by etching troughs down to the nitride layer, leaving the interconnections as tiny bridges over the troughs. This method is similar in principle to the beam lead method of isolation, but preserves the advantage of a rigid substrate.

Samples of these isolation patterns have been prepared (Figure 12) and their isolation measured. It was found to be poor when first tested, but after heat treatment it improved spectacularly. The leakage resistances of cells 1 by 0·75 millimetre were usually between 2×10^{12} and 5×10^{12} ohms at 10 volts, and the knee voltages were between 400 and 500 volts.

6.3.3 *Isolation Using Sapphire Substrates*

Fruitful work on growing epitaxial silicon films on sapphire has been reported recently [5], and mobilities up to half those found in bulk material are claimed.

Such a technique would enable isolation to be obtained simply by depositing a thin epitaxial layer of silicon and then etching an isolation pattern down to the substrate. More-sophisticated arrangements such as that shown in Figure 13 could also be realized. A silicon epitaxial layer is deposited on a sapphire substrate in which shallow depressions have been etched. The silicon is then lapped away until it remains only in isolated islands recessed into the substrate to give a flat surface for interconnections.

At present, a suitable sapphire substrate is expensive, but it is still attractive since much of the processing associated with other isolation methods is avoided, the thermal dissipation is good, and the radio-frequency isolation considerably better.

7. Conclusion

Functional flexibility in microcircuit technique is essential if manufacture is to be decentralized without excessive plant investment. It also enables the advantages of mass production to be applied to the manufacture of special circuits or sub-systems which are not required in very large numbers. It is too early to say if there is any overall advantage in using these techniques for devices such as standard digital circuits, where the numbers are large enough to give a negligible tooling cost per device, and where there are no advantages in decentralized manufacture. In the future, when computer design and layout of circuits are in a more ad-

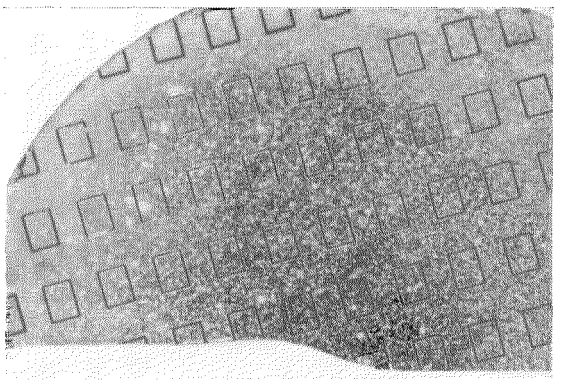


Figure 12—Photograph of dielectric isolation pattern.

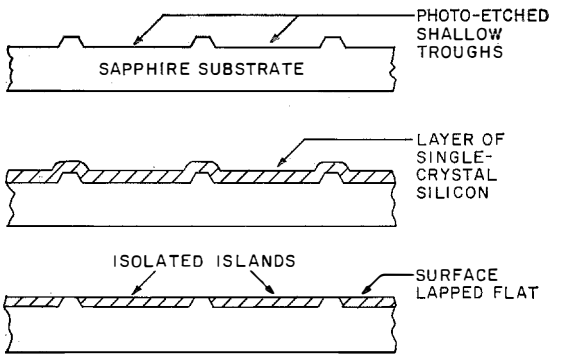


Figure 13—Isolated islands on a sapphire substrate.

vanced stage, the techniques facilitate the direct transition from computer output data to device.

The deposition processes can be separated from function-defining processes for thin-film circuits by the use of the microengraving technique. The former can be used for preparing masks for a 2-dimensional selective etching sequence and for the direct pattern definition of the film components. It has also been adapted for tape control. The time taken to define the function of a typical hybrid circuit is 30 seconds using the automatic system described. Resistor tolerances are ±5 per cent, but with monitoring during microengraving ±0·1 per cent can be obtained. The cellular approach allows resistance-capacitance networks to be defined on universal substrates. The techniques evolved around microengraving are applicable to other micromachining methods such as laser or electron-beam processes when these are further developed.

The extension of the approach to semiconductor integrated circuits has been studied. At present, 3-dimensional processing is not practicable although in the future, ion-beam implantation [6] may provide a means of achieving this. The cellular approach is compatible with the established silicon planar processes. The necessary cell isolation techniques are in an advanced stage of development. Interconnection layouts for cellular universal substrates are readily designed and, except for functions requiring many cross-overs, there is efficient utilization of space. The cutting of interconnection masks on a tape-controlled table has been demonstrated. Full computer circuit design and fabrication, though still in the future, are likely to be more readily applied to the cellular universal substrates than substrates having a random arrangement of components.

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Mr. Horsley is a Graduate Member of the Institution of Electrical Engineers.

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Flip-Chip Semiconductor Devices

P. J. A. McKEOWN
R. D. PEACOCK
STC Semiconductors Ltd.; London, England

1. Introduction

In the development of thin-film circuits, a serious limitation has been the lack of commercially viable thin-film active devices. The need to use conventionally encapsulated transistors and diodes sacrifices much of the space saved by using thin-film and screen-printed circuits. Semiconductor flip-chips suitable for direct mounting have been developed to overcome this problem.

In this paper, a flip-chip device is understood to mean a piece of semiconductor material, normally silicon, containing one or more electronic circuit components and having contact pads on one chip face instead of attached leads. The construction of these permits easy direct attachment of the chip to metal contacts arranged on a plane surface such as a thin-film substrate.

The structure of one of our flip-chip transistors is shown in Figure 1. This shows a section through the active transistor and the emitter and base contacts. The structure is basically that of a silicon planar epitaxial transistor. However, the collector contact which is normally made to the underside of the chip is now made through an additional window cut in the top oxide. It should be appreciated that all the silicon outside the base region is collector. An evaporated pad of metal 0·007 × 0·029 inch (0·178 × 0·737 millimetre) makes ohmic contact to the silicon, and a layer of solder 0·001 inch (0·025 millimetre) thick covers the contact.

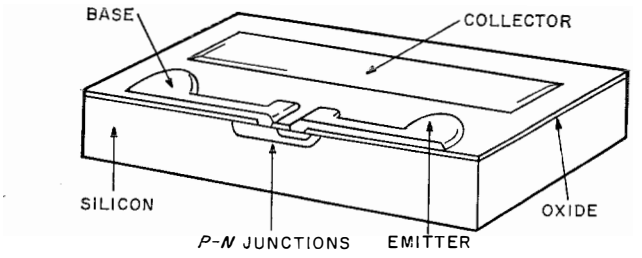

Figure 1—Section through flip-chip transistor.

The emitter and base contacts are similar except that the evaporated metal and solder extend from the holes in the oxide to circular pads 0·007 inch (0·178 millimetre) in diameter well separated from the active area of the device. These pads are electrically insulated from the silicon beneath them by the silicon-dioxide layer grown during planar processing. The circular pads are much larger than the corresponding emitter and base regions of the transistor. This and the large separations of the 3 contact pads greatly facilitate the attachment of the chip to a circuit. With this type of transistor, all the solder required for attachment is provided by the contact pads on the chip.

Unless stated otherwise, the conclusions given elsewhere in this paper refer to the construction described above.

Not all flip-chip devices have this structure. One method of construction [1] has an additional protective layer of glass on top of the silica and uses metal balls as contacts.

2. Technology of Contact Systems

A flip-chip can be said to be mounted successfully to a substrate if the contacts are able to withstand specified environmental and life test conditions, and these conditions must be known before the contact system can be designed to an optimum.

It is clear that the contact system must satisfy the following:—

(A) It must make a good ohmic contact to the silicon through the oxide window.

(B) It must adhere well to the silicon and to the silicon dioxide with high tensile and shear strength.

(C) It should contact the substrate, again with low resistance and high strength.

The contact system developed and used by STC Semiconductors consists of two parts, a vacuum-evaporated metallic layer in contact

with the silicon and silicon dioxide, and a layer of solder in contact with the evaporated layer. The evaporated layer must satisfy **(A)** and **(B)** above and it must make equally good contact with the solder layer.

This evaporated layer is graded from pure chromium in contact with the chip to pure gold for good wetting by the solder [2]. Chromium is chosen for its good adhesion to silicon and silicon dioxide.

The selection of a solder material depends on such factors as the maximum temperature to which the final structure will be subjected, and the wetting properties of the solder to the gold and to the substrate. Eutectic tin/lead and tin/silver are both good contact solders.

2.1 Reducing Contact Failure

It is of interest to consider the potential failure mechanisms and how these can be eliminated or reduced to an acceptable level.

Some weaknesses in the contacts may be due to inadequate control during manufacture. For instance, voids may be formed in the solder unless care is exercised during evaporation. Again, prolonged exposure of thin solderable films to molten solder can lead to solution of part of the film in the solder. Such damage can also be caused by the user when mounting chips.

The formation of a brittle gold/tin compound is known to weaken some soldered joints [3]. This requires an appreciable percentage of gold and has not been observed in flip-chip contacts.

Contact failure resulting from the chemical effects of moisture and flux residues can be eliminated by using a non-activated pure rosin flux for the chip mounting operation and by the exclusion of moisture from the final encapsulated system. Electrochemical effects due to the different metals in the contact system can enhance any chemical attack. A mildly activated flux may be used only if extreme care is taken in the removal of the flux residue.

Finally, it is important to minimize oxidation of the solder during chip storage before assembly.

3. Substrates

The choice of substrate depends on factors such as cost, method of final encapsulation, and environmental conditions during test and use. Typical substrates are printed-circuit board, metallized ceramic, and metallized glass.

Printed-circuit board is convenient as it is readily metallized with copper. However, it must satisfy several rather severe requirements.

Chemical inertness, low moisture absorption, and high temperature resistance are of the utmost importance as well as the more-usual parameters of mechanical strength, etchability, and punching and drilling properties. We use *NEMA* (National Electrical Manufacturers Association) grade 10 glass-fibre/epoxy boards with 1-ounce copper for mounting inside *TO5* encapsulations. For this purpose the interconnection pattern in an array of substrates is etched out using conventional photo-resist techniques and a ferric-chloride etch.

Glass and glazed ceramic are the usual substrate materials for thin-film circuits. A vacuum-evaporated graded gold/chrome layer may be used for the conductors. The interconnection pattern can be defined by evaporation through a mask or by subsequent etching. Figure 2 shows a thin-film circuit with a flip-chip transistor attached.

Glass and ceramic can also be used as substrates for screen-printed interconnections. Platinum/gold resinate inks are often used, and with care, contact pad spacings down to 0·005 inch (0·127 millimetre) can be obtained. High-temperature firing of this screened pattern will result in an adherent metal layer. Thin-film and screen-printing techniques permit the formation of passive components directly on the substrate, and thus only active flip-chips are required to produce complete circuits.

4. Mounting of Flip-Chips

The mounting of a flip-chip device on the chosen substrate is not as straightforward as it may at first appear.

It is necessary first to orientate the chip relative to the substrate interconnection pattern. This can be done by means of orientation marks on the back of the chip as shown in Figure 3. Final positioning of the chip on the substrate contacts is aided by making these contacts as large as possible. It is usually necessary to press the chip to ensure that the solder "bumps" are in good contact with the substrate contact pads. This is of particular importance in the case of chips with more than three contacts, as it is possible for the bumps to be of slightly different thicknesses.

Fluxing is usually necessary, although the extent of this and the type of flux required will depend on the substrate preparation and the method of applying heat to the assembly.

With printed-circuit board it is best to etch the copper interconnection pattern lightly with a ferric-chloride etch just before the soldering operation. This pre-cleaning is not required with evaporated and fired screen-printed noble-metal interconnections. Fluxes may be mildly activated organic acid or rosin types.

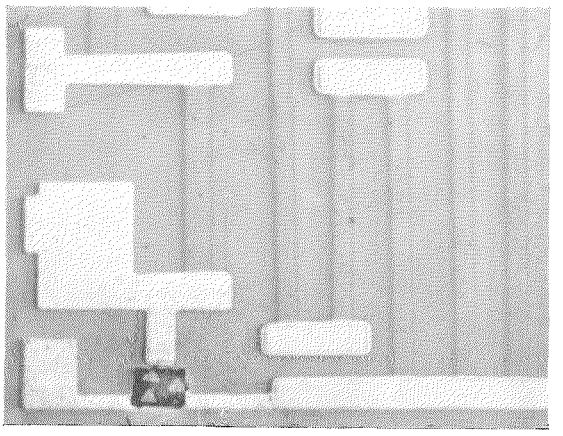

Figure 2—Thin-film circuit with a flip-chip transistor attached at bottom.

It is unwise to assume that halide activators are completely broken down during the heat cycle, or that other organic acids which may be present are inert. The best practice with this kind of flux is to use a short soldering time cycle and then to remove thoroughly all residues by Soxhlet extraction using a solvent such as isopropyl alcohol.

Pure water-white rosin flux is inert [4, 5] but its relative inactivity can make it difficult to use unless all components are thoroughly clean. This is the preferred flux for high reliability.

The soldering operation should be done at the lowest temperature consistent with good wetting of the substrate contact and for the shortest time. This will minimize possible scavenging of the substrate contact material (in the case of metallized ceramic and glass) and dewetting of the chromium layer on the chip. A convenient

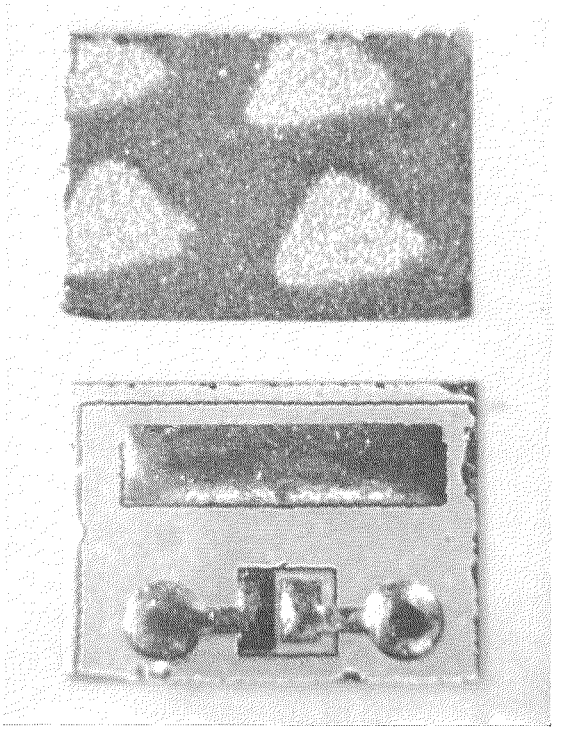

Figure 3—Flip-chip transistors showing contacts and orientation triangles.

technique is to use a conveyer-belt furnace although it is difficult to satisfy the minimum time requirement. It is desirable to maintain pressure on the chip during the soldering cycle to prevent the chip from floating on the flux or solder. This can lead to weak joints or open circuits. Jigging to do this with a conveyor is complex, especially if a number of chips of different sizes and thicknesses are to be soldered down simultaneously.

A better way is to solder each chip individually under pressure. In the case of a thin-film glass or ceramic substrate, heat can easily be applied under the substrate, and the chip need only be positioned and held down with a weighted probe for the duration of the soldering cycle. Pre-heating of the substrate will sometimes help to minimize thermal shock. For low-thermal-conductivity substrate such as printed-circuit board, the weighted probe itself must be heated. Electric heating with thermocouple control is convenient.

It is good practice to space the chip away from the substrate so that the silicon at the edge of the chip cannot be short-circuited to the substrate. This can readily be done with printed-circuit board by etching out the interconnection to leave raised pads of copper ready to receive the chip contacts as shown in Figure 4.

Other possible techniques consist of depositing a layer of glass on the contact side of the chip to increase the distance between the silicon and the solder [1]. In the case of printed-circuit board, the substrate interconnections can be heavily oxidized in all regions except the contact pads. The solder will then wet only the clean pads. Deposited layers of material which is not wet by solder can be used to restrict solder flow on thin-film and screen-printed circuits.

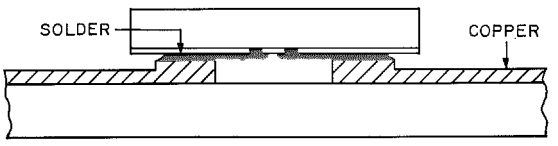

Figure 4—Chip mounted on copper-clad printed-circuit board.

The fully assembled flip-chip circuit must finally be encapsulated. A printed-circuit board or ceramic disc will fit over the pins of a 10- or 8-lead *TO5* header, and the circuit terminations can be soldered directly to these pins as shown in Figure 5. Circuits in which all active and passive components are in chip form are known as multichip circuits. For thin-film and screen-printed circuits, a flat package is more commonly used than a *TO5*.

The solder contacts are normally strong enough to hold the chip in place. If a plastic-filled encapsulation is required, the layer in contact with the chips should be chosen so that no stress is built up in curing or subsequent use.

5. Characteristics of Flip-Chip Devices

At the time of writing, many manufacturers are developing flip-chip devices with solder contacts but only a few (Standard Telephones and Cables, Hughes Aircraft Company, and Semiconductors Limited) are selling individual chips. The range of devices is limited but is increasing. Most transistors are *n-p-n* but we have developed a *p-n-p* type. Gains and voltage ratings are typical of low-level silicon planar devices. $V_{CE(sat)}$ is typically 0·2 to 0·25 volt at 10 milliamperes. Leakage currents on the chip are similar to those of conventional devices, but the values obtained after mounting may depend mainly on the method of mounting and the thoroughness of flux removal. A limitation at present exists in high-frequency performance; f_T is normally about 300 megahertz. Very-high-frequency operation could be limited in part by the contact–silicon capacitance, which typically amounts to 0·5 to 1 picofarad per contact. Power dissipation is also limited by the low thermal conductivity of many substrates and the limited area of contact between chip and substrate. A maximum of 200 milliwatts at 25 degrees Celsius ambient is typical for tran-

sistors and 100 milliwatts for diodes. The maximum operating temperatures are usually about 60 degrees Celsius below the melting point of the solder employed, but will of course depend on the nature of the substrate.

6. Reliability of Flip-Chip Devices

As the introduction of flip-chip devices is relatively recent, little reliability information has been published. The first results of a major government-sponsored reliability programme on flip-chips, being conducted by STC Semiconductors, are now available.

In addition to the obvious examination of catastrophic failures including intermittent failures, certain sensitive characteristics have been chosen to detect degradation. These are V_{CES} to detect any increase in contact resistance, I_{CBO} which is sensitive to any failure of the oxide passivation as well as leakage through flux deposits, and h_{fe} as a general monitor and to detect large stresses in the transistor structure.

The mechanical reliability of flip-chip mounted devices is the most obvious concern. Centrifuging to 18 000g in the direction tending to pull chips from the substrate has no effect. Indeed, a pull of 600 grammes is required to remove a typical transistor chip of the type shown in Figure 1. This corresponds to an acceleration of 1 800 000g. There is little difference in this respect between tin/lead and tin/silver contacts. The shear force required to remove a chip is about 500 grammes. Another convenient mechanical test has been to drop encapsulated multichip circuits (Figure 5) 16 inches (0·4 metre) on to a steel plate. The chips of these circuits are not embedded in any protective plastic, yet results show no failure or degradation in 48 devices after 20 000 drops. There are, however, some subtle causes of mechanical unreliability. Flexure of the substrate can cause failure or weakening of the contacts, particularly when using large chips containing monolithic circuits. In one experiment, devices which had been stressed in this way showed a failure rate of 57 per cent when subjected to a shortened version (1200 drops) of the drop test described above.

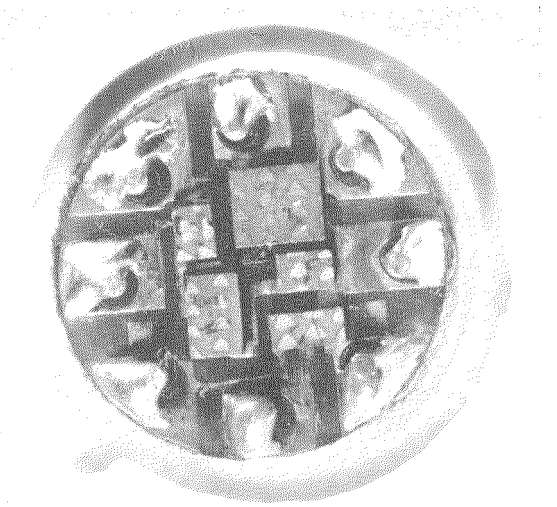

Figure 5—Multichip circuit on *TO5* header before encapsulation.

The failure rate of flip-chips under conditions of high-temperature storage has been measured under dry conditions. 220 chips with tin/lead contacts stored at 130 degrees Celsius for 500 hours show no catastrophic failures or change in V_{CES}. Initial experiments with 28 devices having tin/silver contacts show no failures or degradation in 1000 hours. Similar results are obtained with temperature cycling. Five cycles between −55 and +125 degrees Celsius result in no failure or degradation among 50 chips with tin/lead contacts and 50 with tin/silver contacts mounted on printed-circuit board.

The effect of electrical stress on chip reliability appears to be small within the specified voltage and power limits. An initial experiment has shown one failure in 20 000 device-hours at 75 degrees Celsius with dry ambient (relative humidity = 0 per cent) and a switching frequency of 1 megahertz. International Business Machines [1] has shown zero failures in 48 devices electrically cycled between 85 and 150

degrees Celsius for 5000 hours. However, storage at 150 degrees Celsius with reverse bias for 500 hours resulted in 3 failures out of 89.

Humidity has a degrading effect on reliability. Chips with tin/lead contacts, in steam at one atmosphere pressure at 135 degrees Celsius, have a mean life of about 2000 hours. This contrasts markedly with the results at a relative humidity of 0 percent noted above. Increases in V_{CES} are also noted after exposure to extremes of humidity and temperature. The average chip life is much greater at lower temperatures. The activation energy of the degradation mechanism is 1500 calories per mole at 135 degrees Celsius and decreases at lower temperatures. Tin/silver contacts show a substantial improvement in resistance to the effects of humidity.

Humidity tests [1] show zero failures in 99 devices at 85 degrees Celsius and relative humidity of 85 per cent, with reverse bias for 5000 hours.

7. Current Trends

Most examples of flip-chip technology to date have been based on the flip-chip transistor with integral solder contacts. Two major developments, aluminium contacts and flip-chip monolithics, have begun to alter this state of affairs.

The extension of the flip-chip technique to monolithic circuits is an obvious step since special bonding pads are already provided around the periphery of the chip [6].

Monolithic circuits with solder contacts have been made by STC Semiconductors. Monolithic chips with soldered copper ball contacts have been described [7]. However, most of the reported examples of flip-chip monolithics have had weldable contacts.

Microelectronic circuits are constantly being pushed to higher operating temperatures and lower costs. The use of solder limits the temperature and the special solderable metallization does not make for minimum cost. Of the contact materials with higher melting points, aluminium is an obvious choice since it is widely used for semiconductor contacts and permits the use of an all-aluminium contact system. Attachment by means of sonowelding has been shown to be feasible [8]. This technique permits the use of normal monolithic chips.

To minimize short-circuits and allow for some lack of planarity in chip and substrate, thick contact pads are normally used to space the chip away from the main substrate. These are formed initially on the substrate. The build up of pads on the chip has been reported [9]. The attachment of a chip to a kovar lead frame instead of a glass or ceramic substrate is another recent development [10].

Not all weldable contacts are aluminium. A unique contact system employing gold leads, which project beyond the edges of the chip and can be used for flip-chip mounting, has been developed by Bell Telephone Laboratories [11].

Apart from techniques of mounting chips, flip-chip developments are to be expected in at least the two areas of parasitic capacitance and power dissipation. More attention may be paid to thickening the dielectric between pads and silicon, and also to isolating the underlying silicon. Improvements are also to be expected in the heat-sink properties of contacts, dielectric, and substrate.

8. Acknowledgment

The authors would like to thank the United Kingdom Ministry of Defence for permission to quote reliability results obtained under contract CP 6687/59.

9. References

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Patrick J. A. McKeown was born in Coleraine, Northern Ireland, in 1928. He received a Bachelor of Science degree in chemistry from Queens University, Belfast, in 1948 and Master of Science and Doctor of Philosophy degrees in X-ray crystallography in 1950 and 1954 respectively.

He joined the Department of Chemical Engineering, Imperial College, London, as Assistant Lecturer in 1954. In 1957 he joined the Transistor Division of Standard Telephones and Cables where he is now responsible for integrated-circuit engineering. He has written papers on crystallography, instrumentation, semiconductor processing, and integrated circuits.

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Robert David Peacock was born in London in 1930. He obtained a Higher National Certificate in Electrical Engineering at the North West Kent College of Technology in 1960 and has a City and Guilds of London Institute Bronze Medal in Photography.

He joined the Semiconductor Division of Associated Electrical Industries in 1956 and worked on germanium alloy transistors, germanium diodes, and silicon rectifiers. In 1959 he joined the Transistor Division of Standard Telephones and Cables and was responsible for the development of germanium ultra-high-frequency mesa transistors. He is now responsible for all mask-making activities, development of multichip contact systems, and development of monolithic integrated circuits.

Silicon Integrated Circuits

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1. Digital Integrated Circuits

1.1 Diode Logic

Any logic expression can be satisfied with diodes as long as no storage or inversion is necessary. A typical AND gate is shown in Figure 1.

Here, if all inputs (A and B and C) are high, the output will be high ($D = ABC$). This is called positive AND logic because in a system having only two voltage states (a positive or high voltage and a negative or low voltage) it is in reference to the positive voltage. This same circuit could be an OR circuit if we used a low voltage as reference by saying the output would be low if any of the inputs were low, and it would then be negative OR logic.

A positive OR (negative AND) gate is shown in Figure 2. If any input (A or B or C) is high, the output will be high ($D = A + B + C$). These two gates are sufficient to satisfy all logic expressions.

It probably is not possible to build a computer with only these two gates because most problems cannot be solved effectively without inverters.

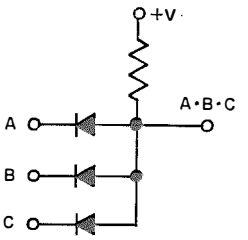

Figure 1—Diode positive AND gate.

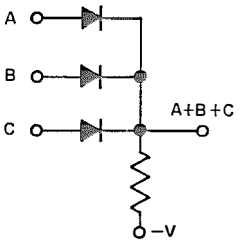

Figure 2—Diode positive OR gate.

1.2 Diode-Transistor Logic

Transistor inverters are necessary with diode gates. One type of diode-transistor logic (DTL) is shown in Figure 3. This is the AND circuit of Figure 1 coupled to an inverter. It is called the NAND circuit (NOT AND). It will satisfy all logic expressions and also invert.

Another circuit which is sufficient for all functions in a computer is the NOR (NOT OR) circuit. Like the NAND circuit, it is a diode OR connected to an inverter. See Figure 4.

The positive NAND circuit (Figure 3) is a negative NOR. Likewise, the positive NOR is a negative NAND.

1.3 All-Transistor Logic

The oldest form of all-transistor logic is direct-coupled-transistor logic ($DCTL$) shown in Figure 5. A modification of this with a resistor

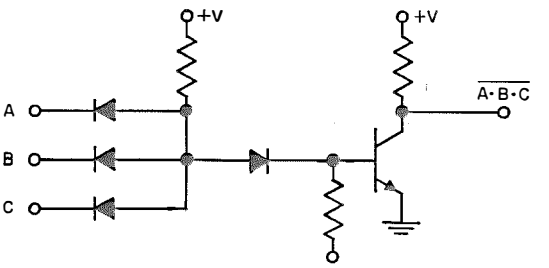

Figure 3—Diode-transistor-logic NAND gate.

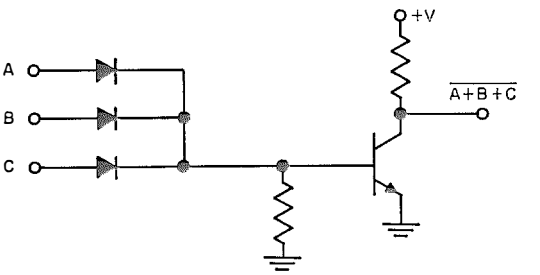

Figure 4—Diode-transistor-logic NOR gate.

in each base is shown in Figure 6. This is often called resistor-transistor logic (RTL) to avoid the connotation of direct-coupled-transistor logic ($DCTL$). A further modification with a speed-up capacitor shown in Figure 7 is resistor-capacitor-transistor logic ($RCTL$). These three all-transistor circuits are NOR circuits.

Another all-transistor NOR circuit is the current-mode-logic (CML) circuit shown in Figure 8.

One of the most recent types of logic is the transistor-transistor logic (T^2L) in Figure 9. It is a NAND circuit.

Since $Q = VC$, circuits with small voltage swings require less parasitic charge. Also, circuits with lower thresholds require less charge. Nonsaturated circuits require less charge because there are no excess minority carriers.

This looks like a simple set of rules to live with except that there are other performance requirements that contradict these. In general, all of the things that make a circuit need less charge also make it less likely to be able to supply that charge to other circuits. A circuit that requires less charge is more susceptible to

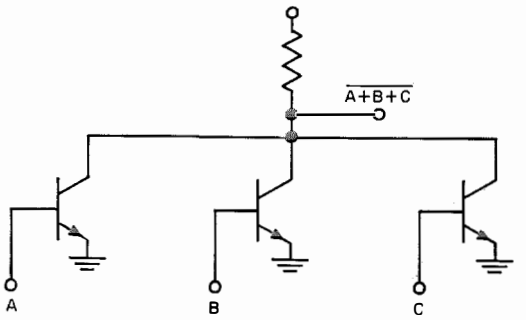

Figure 5—Direct-coupled-transistor logic.

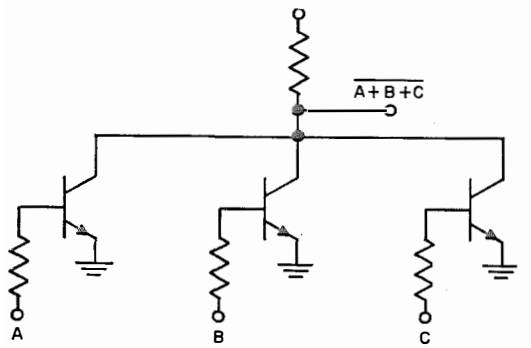

Figure 6—Modified direct-coupled-transistor logic.

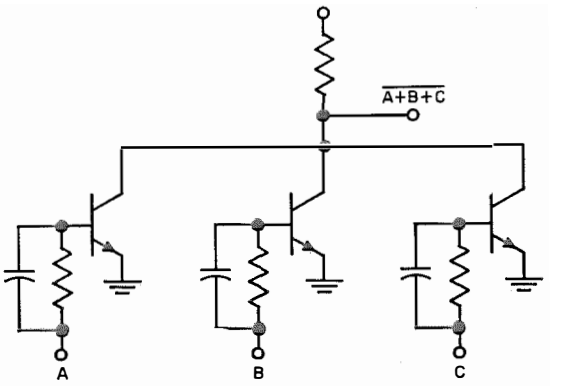

Figure 7—Resistor-capacitor-transistor logic.

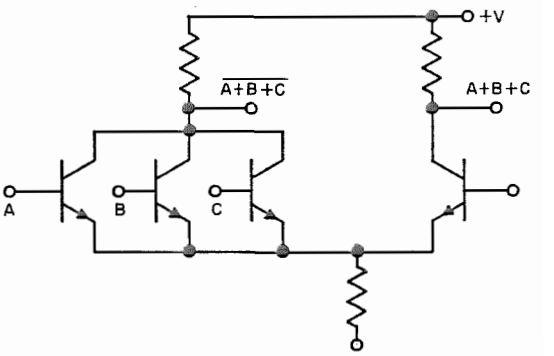

Figure 8—Current-mode logic.

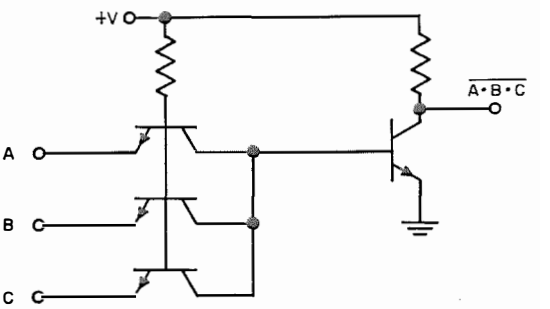

Figure 9—Transistor-transistor logic.

noise charge. Circuits with small voltage swings require closer matching of components.

It is possible to amplify a charge with a transistor, but this adds propagation time because of transit time in the base. If the transistor is an inverter, it takes even more time because of inverse feedback. With all integrated circuits, there is inverse feedback from components besides that within the transistors. The circuits above that have inverters are all charge amplifiers. An example of a noninverting charge amplifier is the emitter-follower. The circuit in Figure 10 performs the same function as the circuit in Figure 1 except that it will amplify current and charge ($Q = \int idt$). (Our *300* Series is this type of modified diode-transistor logic. The Fairchild complementary transistor logic (*CTL*) is much the same).

The switching speed of the diode gates themselves can be made quite fast because the parasitic capacitance and excess-minority-carrier effect can be made small. The diode AND gate of Figure 1, when connected to an inverter, becomes the diode-transistor-logic NAND gate of Figure 3, which is much slower. The transistor-transistor-logic NAND gate is faster than the diode-transistor-logic gate because it will pull charge out of the inverter faster. It still is slower than the diode gate.

The direct-coupled-transistor logic and resistance-capacitance-transistor logic in Figures 5 and 7 can be as fast as the transistor-transistor logic under certain conditions. The modified direct-coupled-transistor logic in Figure 6 is slightly slower because the base resistors limit the rate of supplying charge.

The current-mode-logic circuit in Figure 8 is a nonsaturating circuit and therefore has no problems with excess minority carriers. It is the fastest of the inverting circuits but not as fast as the diode circuits.

We see the relative charge requirements of these circuits. However, their ability to supply charge is at least as important because in a large computer the parasitic charge necessary for wiring capacitance can be 10 times that of the circuit being driven. The ability to supply charge depends on the output impedance. On all the circuits except the current-mode logic and the noninverting diode gates, the output part of the circuit is a saturated transistor. The impedance will be low when turning on but the load resistor must supply the charge when turning off. The diode circuits are similar except that the diodes add some resistance. The current-mode-logic circuits usually have somewhat higher impedance when turning on because they don't saturate; however, the load resistor is somewhat smaller, which gives a lower impedance when turning off.

The trend in integrated circuits is to go to a multitransistor inverter that has low impedance

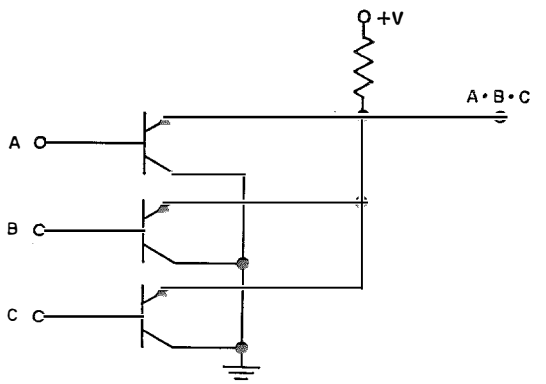

Figure 10—Transistor AND gate.

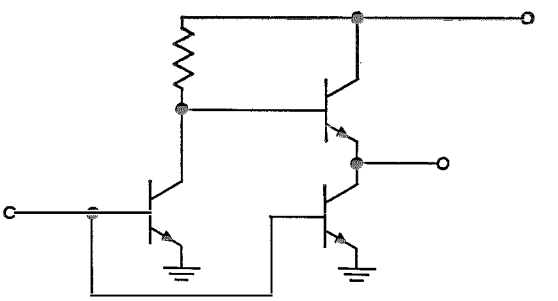

Figure 11—Low-impedance inverter.

both ways, such as the one in Figure 11 which is used in our *300* Series.

1.4 Thresholds and Noise Margin

Recently, the military suppliers have been stressing circuits with good noise margin. The way the noise is defined, it is a voltage appearing on any terminal. Of the circuits mentioned here, diode-transistor logic has the best noise margin; however, extra noise margin can be added to any of the circuits by adding diodes or transistors in series to increase threshold voltage. It would also make larger voltage swings necessary and more parasitic charge would have to be supplied. The extra diodes or transistors may also degrade switching speeds; for instance, the transistor-transistor-logic gate probably would lose its speed advantage because it would no longer be effective in getting charge out of the inverter.

An interesting combination of the transistor-transistor-logic gate with a large noise margin and low output impedance is shown in Figure 12. This circuit is used widely in the *TFX* (*F111*) aircraft and is supplied by many manufacturers. It is the only transistor-transistor-logic circuit known by many people and, for that reason, they associate this logic with good noise margin and low output impedance. Here, most of the advantages of the transistor-transistor-logic inputs are lost because Q1 is in series with Q2 and Q3. Some of the gates in our diode-transistor-logic line are quite similar except that they have diode inputs.

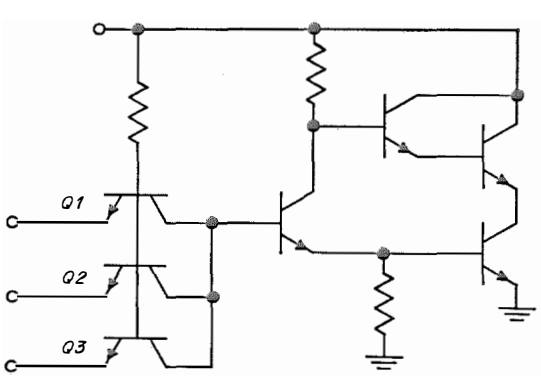

Figure 12—Gate used extensively in equipment for the *TFX* (*F111*) aircraft.

1.5 Standards of Logic

The basic Boolean algebra built around relays used AND-OR logic. It can be shown that all logic expressions can be reduced to a 2-level expression of a number of AND gates fanning in to a single OR gate. This is a minterm expression and is all-inclusive. There is also a reduced form which is all-exclusive called a maxterm expression. It would include a number of OR gates fanning in to a single AND gate. Combining AND, OR, NAND, and NOR, there are 8 standards.

Minterm	*Maxterm*
AND/OR	OR/AND
NAND/NAND	NOR/NOR
OR/NAND	AND/NOR
NOR/OR	NAND/AND

Generally speaking, the all-inclusive minterm expressions are easier to handle because we normally think of doing things rather than not doing things. It is quite easy to transform expressions within the maxterm or minterm groups, but quite difficult to transform from one to the other. If a system is built around one form, the usual way of changing to the other is by using inverse logic connotation, which makes maxterms become minterms or vice versa without changing the circuit.

1.6 Component Tolerance

In Figure 13, the possible fanout for a varying coupling resistor is shown for a simple circuit using typical silicon transistors with other circuit parameters held constant. Similar curves can be drawn for other circuits and with other variables. Integrated circuits with the widest possible parameter spread are the easiest to build. Designs with spread of ±20 percent in almost any parameter are quite common. It is extremely difficult to build a circuit if the

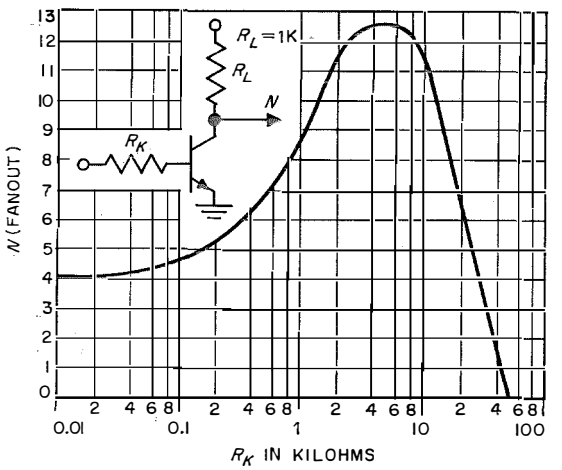

Figure 13—Fanout for a varying coupling resistor.

customer specifies the tolerance of the component parameter. Often, these component measurements are impossible to make. The customer should specify black-box performance.

Table 1 lists important logic types and their major characteristics. The relative speed is for a given power dissipation and a given transistor type. Actually, any one of these circuits can have an advantage depending on how it is used.

All of these integrated circuits were designed for the military market and the table refers to that market in the column on customer acceptance. Diode-transistor logic is fairly well accepted in industrial applications and in peripheral equipment for commercial computers. Current-mode logic is gaining acceptance in the high-speed portions of commercial computers.

1.7 Industrial Digital Circuits

Many industrial requirements are for good noise-charge immunity as well as noise-voltage immunity. This calls for new circuits that will probably have the performance of a transistor-resistor-logic circuit but will not use resistor logic because that would require close tolerance.

Metal-oxide-semiconductor (*MOS*) approaches to the industrial market have created much interest in recent months. Their noise-charge immunity is poor. Also, there is no significant difference in possible complexity compared with bipolar integrated circuits if high impedance (low power) is not necessary. The difference in manufacturing cost does not appear significant. Metal-oxide semiconductors can be considered another tool for all types of integrated circuits and will be used in products that need its properties and characteristics.

1.8 Commercial-Computer Integrated Circuits

Several commercial computers are being built using current-mode logic. The circuit configurations leave much to be desired, and improved current-mode-logic designs may be expected.

TABLE 1
Important Logic Types

Type of Logic	Propagation Time (Relative)	Noise Margin	Ease of Manufacturing	Customer Acceptance
Diode	X	Good	Good	Good
Modified diode	$0.5X$	Good	Good	Good
Diode-transistor (*DTL*)	$4X$	Good	Good	Excellent
Direct-coupled-transistor (*DCTL*)	$3X$	Poor	Good	Poor
Modified *DCTL* or resistor-transistor (*RTL*)	$4X$	Fair	Excellent	Fair
Resistor-capacitor-transistor (*RCTL*)	$4X$	Fair	Excellent	Fair
Transistor-transistor (T^2L) (Figure 9)	$3X$	Fair	Poor	Good
Transistor-transistor (T^2L) (Figure 12)	$3.5X$	Good	Fair	Excellent
Current-mode (*CML*)	$2X$	Poor	Poor	Poor

2. Linear Integrated Circuits

Full advantages of integrated-circuit construction and operation can be best realized if the complete circuit required for a particular application is contained within a single package with as few external components as possible. Monolithic construction is more desirable than multichip or hybrid packages.

Integrated circuits are available with various degrees of linear circuit development, ranging from individual passive or active circuit components that require extensive external circuits through complete functional circuits that require only external connections for the signal input and output and the direct-current supply voltage.

2.1 Operational Amplifiers

Operational amplifiers come close to being a universal amplifier. For this reason, integrated-circuit manufacturers started making these first. Almost always, external components were used with them to set the characteristics. In fact, the versatility is based on the wide range of circuit characteristics that can be set with a few external components.

Figure 14 is an operational amplifier integrated circuit. It uses *n-p-n* and *p-n-p* transistors. The double-ended input makes the device capable of comparing voltage levels, which is another desirable feature. This is a direct-current amplifier with gain of about 60 decibels up to about 100 kilohertz.

Figure 15 shows an operational amplifier using only *n-p-n* transistors. Its characteristics are

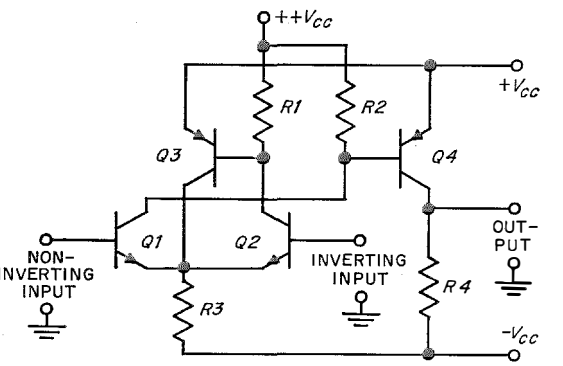

Figure 14—Operational amplifier integrated circuit.

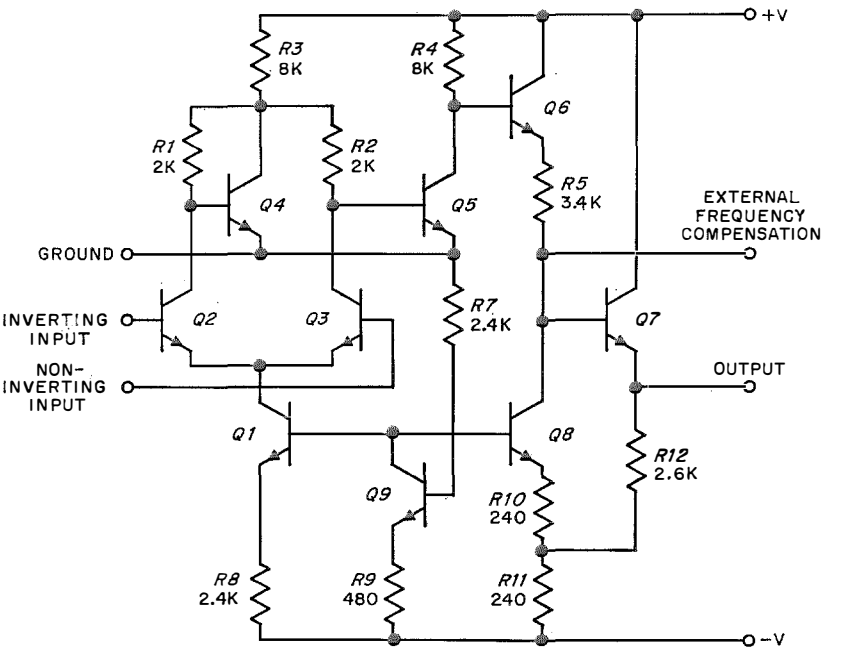

Figure 15—Integrated-circuit operational amplifier using *n-p-n* transistors.

much like the one above except that the bandwidth is greater.

A number of applications suggested for operational amplifiers follow.

(A) Transformerless modulator-demodulator
(B) Delay equalizer
(C) Zero-crossing detector
(D) Nuclear reactor bistable trip
(E) Sweep generator for pulse-position indicator
(F) Preamplifier for servo system using solar-cell sensors
(G) Thermistor bridge amplifier
(H) High-speed photodiode amplifier
(I) Band-pass amplifier using a twin-*T* bridge
(J) High-input-impedance amplifier for a piezoelectric transducer
(K) Integrator or low-pass amplifier
(L) Half-wave rectifier
(M) Peak detector
(N) Voltage follower
(O) Clamper
(P) Peak-to-peak detector
(Q) Full-wave rectifier
(R) Transformerless 400-hertz phase detector.

2.2 Hearing-Aid Amplifiers

The first consumer integrated circuit was the hearing-aid amplifier shown in Figure 16. This was a reasonable development, as hearing-aid users are willing to pay a premium for minimum size and weight.

2.3 Radio-Frequency and Intermediate-Frequency Amplifiers

Almost all radio-frequency and intermediate-frequency amplifiers constructed with conventional components use inductance-capacitance networks for obtaining frequency selectivity and establishing band-pass characteristics. The high-*Q* inductors used in these conventional circuits are not available at this time in integrated-circuit form. Methods for obtaining frequency selectivity, when using integrated circuits, are as follows.

(A) The active devices and other parts of the circuit may be constructed in integrated form and connected to conventional inductance-capacitance, resistance-capacitance, ceramic, or crystal filters mounted outside the network package.

(B) Resistance-capacitance filters may be constructed as a portion of the integrated circuit or constructed on a separate substrate and mounted outside the network package.

(C) Resistance-capacitance digital types of filter systems may be constructed in network form as a portion of the integrated circuit.

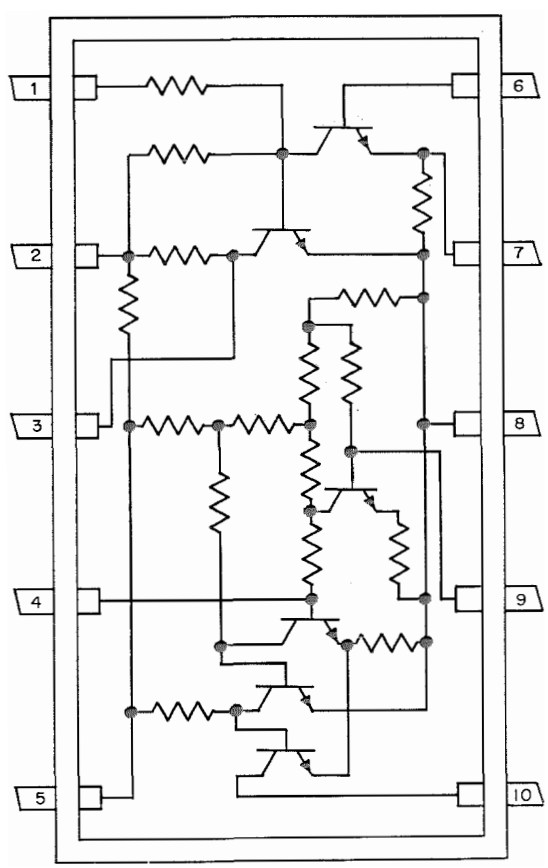

Figure 16—Hearing-aid amplifier.

Resistance-capacitance networks, consisting essentially of combinations of high-pass and low-pass filters, have been used for years in low-frequency oscillator circuits. These circuits may take the form of a Wien bridge, as shown in Figure 17, or they may take the form of a twin-T network as illustrated in Figure 18.

Another frequency-selective circuit, containing a resistor shunted by a lumped capacitance C and a distributed capacitance to ground C_d, is shown in Figure 19.

Note that the resistor in combination with the distributed capacitance to ground forms a low-pass filter, and the resistor in combination with the lumped capacitance forms a high-pass filter.

A differential-type amplifier is well suited for radio-frequency and intermediate-frequency applications because of the ease with which the amplification may be varied with a direct-current automatic-gain-control voltage. In Figure 20, Q1 is operated in the common-collector connection and is driving a common-base amplifier, Q2. The common-base input impedance of Q2 is very low (perhaps 50 ohms), compared with R_E. Therefore, the input impedance of Q2 is essentially the load impedance driven by Q1. If the direct-current voltage $-V_{EE}$ connected to R_E is large compared with the base-to-emitter voltages of Q1 and Q2, the collector currents of Q1 and Q2 will be determined by $-V_{EE}$ and R_E. The voltage amplification of this circuit may be controlled by varying the direct-current collector currents of Q1 and Q2 as a result of changing the negative direct-current supply voltage $-V_{EE}$.

The output-voltage-versus-input-voltage characteristics of this amplifier are illustrated in Figure 21.

Note that if the direct-current resistance of Z_L is small, the direct-current collector voltage of Q2 will be essentially unchanged as $-V_{EE}$ is varied. Therefore, the amplifier will not be detuned because of changes in transistor collector capacitance as the amplification is varied.

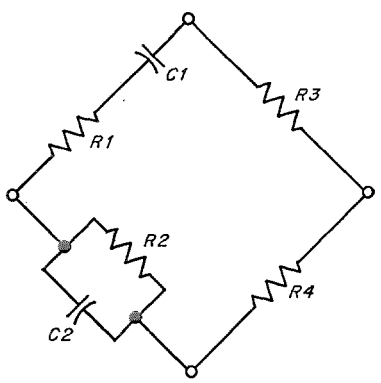

Figure 17—Wien bridge network.

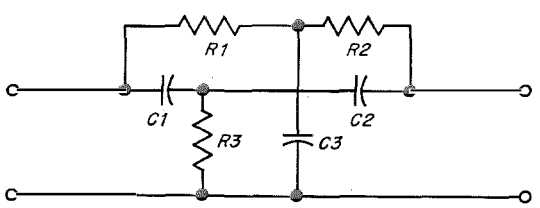

Figure 18—Twin-T network.

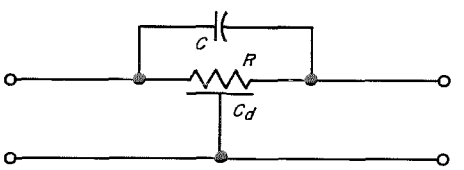

Figure 19—Distributed-capacitance resistance-capacitance filter.

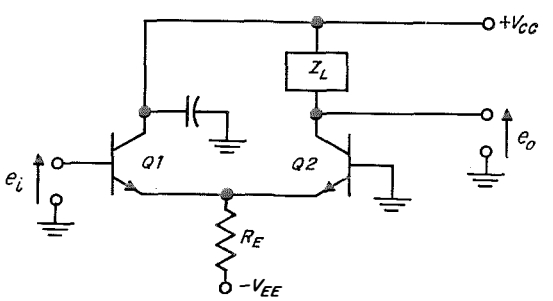

Figure 20—Differential-type amplifier circuit for use as a radio-frequency amplifier.

The circuit diagram of a 600-kilohertz differential-type amplifier with automatic gain control is shown in Figure 22. The range of automatic gain control is about 40 decibels. This integrated circuit uses external inductance components for band-pass filtering.

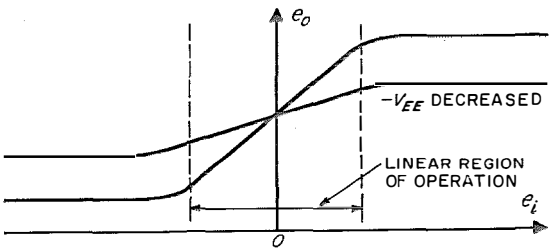

Figure 21—Effect on the e_o-e_i transfer characteristic due to changing $-V_{EE}$.

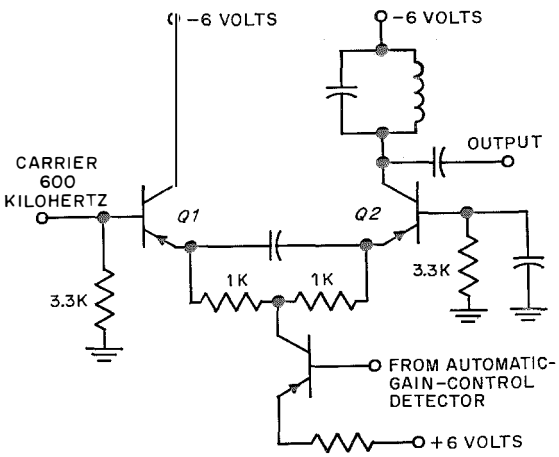

Figure 22—Differential-type amplifier with automatic gain control.

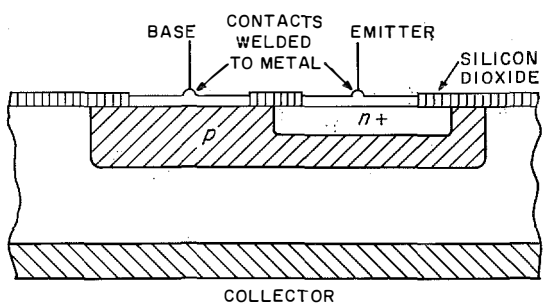

Figure 23—Planar n-p-n transistor.

2.4 Power Amplifiers

The connotation of power includes devices operating up to 1 ampere. Above that level there is little advantage in integrated circuits over the use of power transistors.

3. Integrated-Circuit Fabrication

3.1 Process Techniques

Integrated-circuit processing differs from planar-transistor processing only in the method of isolating components. Figure 23 shows a cross section of an n-p-n planar transistor. An n-type starting material is used with a subsequent p-type base diffusion and n-type emitter diffusion.

The first planar integrated circuits were made with all-diffused processes. One common approach is to diffuse an n-type collector into a p-type starting material with subsequent base and emitter diffusion as in planar transistors. The extra diffusion is necessary to isolate collectors from each other (see Figure 24). Another all-diffusion technique is to start with an n-type material and diffuse p-type selectively

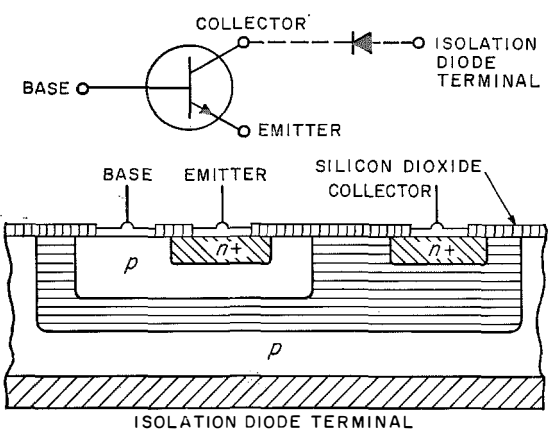

Figure 24—Planar n-p-n transistor on integrated-circuit structure.

from one surface and all over from the back. When the diffusions meet in the center, *n*-type islands will be left which would represent collectors of the transistors in the integrated circuits.

Both of the above all-diffused processes leave something to be desired. They have extremely long diffusion times and sometimes require extremely thin slices. They don't give optimum transistor characteristics.

The next approach was to start with a *p*-type substrate, grow a thin *n*-type epitaxial layer, and selectively diffuse *p*-type down to the *p* substrate to separate the transistor collectors. The cross section would still look like that in Figure 24. The transistor characteristic which was hardest to control with any of these processes was the effective series resistance of the collector.

Two approaches have been used to upgrade the transistor characteristics. The first is to start with a *p*-type substrate, selectively diffuse a high-concentration *n* layer into the substrate, and then grow a lower-concentration epitaxial layer. Isolation is accomplished by a *p*-type diffusion from the top (see Figure 25).

The other approach is to start with a *p*-type substrate and grow a thin *n*+ epitaxial layer with a subsequent low-concentration *n* epitaxial layer. The isolation is performed with a high-concentration *p*-type diffusion from the surface (see Figure 26).

Transistors built with both of these processes have about the same characteristics. However, the diffused layer under epitaxy is easier to isolate with higher breakdown voltages even though it has a few more process steps. On the other hand, the double epitaxial approach allows buying starting material with the epitaxial growth already performed.

Within the past year or two, most manufacturers of integrated circuits have been working on a process that isolates components with silicon dioxide. The approach is to etch islands in an *n*-type piece of silicon, giving it a waffle-like appearance. An oxide is then grown on the waffle, and polycrystal silicon is subsequently grown on the same side. The next step is to lap from the *n*-type side down to the exposed silicon dioxide between the islands. This now gives a planar surface with isolated islands where components can be formed.

The processes for manufacturing integrated circuits are set for transistor characteristics. At the same time, resistors and capacitors can be formed using the same steps. For instance, the base diffusion is also the resistor diffusion. A capacitor is only a large transistor using the capacitance of that large junction.

3.2 Packaging

Most integrated circuits are packaged using techniques that were developed for transistor manufacture. This includes an initial header of suitable size and shape with either gold or

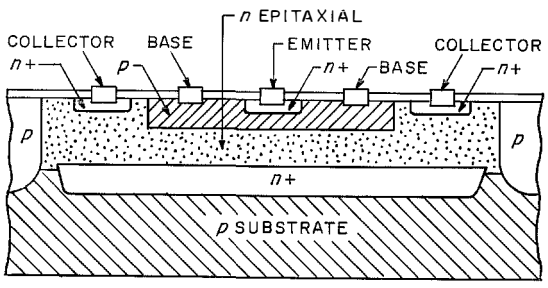

Figure 25—Cross section showing *n*+ diffusion under the epitaxial layer.

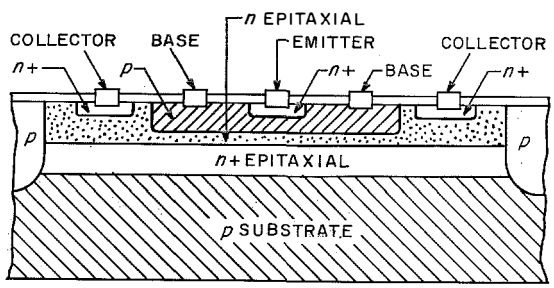

Figure 26—Cross section of double epitaxial layer.

aluminum wires bonded from dice to the header leads. Then a lid is applied to the header either by welding, soldering, or glazing.

The most popular types of packages have been multilead *TO5* headers and flat packs. There have been some recent developments in integrated-circuit packages that are more consistent with integrated-circuit processes.

Figure 27 shows a packaging approach based on integrated-circuit techniques. The leads are bonded directly to the silicon die, and preglazed lids are molded around the lead-and-die assembly in a voiless construction. A vertical-lead version may also be used. Glass can be the sealant, but once bonded others could be employed such as epoxy. Such packaging could significantly reduce the cost of integrated circuits.

3.3 Testing

Digital integrated circuits are usually tested under worst-case conditions. They are treated as a black box relating output characteristics to input requirements. There are several high-speed automatic testers available that can do about 50 tests in a few milliseconds.

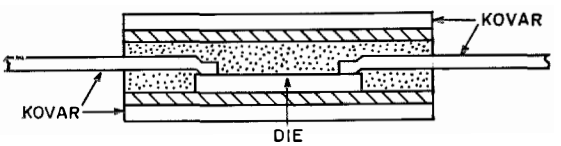

Figure 27—Packaging method.

Analog circuits are presently being produced in small volumes that cannot justify automatic test equipment. Also, some circuits are high-gain amplifiers and require some kind of adjustment during assembly to set their stability. This adjustment and a complicated test setup are the primary cause of high cost.

3.4 Quality Control

Quality control is a functional tool in integrated-circuit manufacture. There are so many process steps that independent monitoring is necessary to catch process breakdown before it significantly affects the product. Since most integrated circuits still go into military equipment, quality control is a very important manufacturing requirement to the customer.

Quality control involves inspection in-line after all oxides are removed and during assembly processing. It includes lot traceability and accelerated life test with periodic add-to as required by Specifications *Mil 9858A* and *NASA 19-500*.

C. R. Cook was born in Buffalo, New York, on 28 July 1932. After service in the United States Marine Corps, he received a bachelor's degree in electrical engineering from Georgia Institute of Technology.

In 1958 he joined Texas Instruments, where he later became a member of its first group on integrated circuits.

In 1964 he came to ITT Semiconductors and is now director of research and development of integrated circuits.

Mr. Cook is a Member of the Institute of Electrical and Electronics Engineers.

Sandwich-Type Structure Providing Novel Resistor Configurations

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ITT Semiconductors; Palo Alto, California

1. Introduction

The technology of integrated microcircuits has encountered a contradiction of physical realizability. Because of advancements in the state of the art of semiconductor-device technology, it is now possible to produce transistors occupying a space of only 1 square mil. Based on these devices, integrated microcircuits are being designed which will dissipate only microwatts of power [1–3].

The method of obtaining this low-power operation is to use resistances in the vicinity of megohms, low terminal voltages, and hence very low currents. The required values of these resistor networks are so large that diffused monolithic resistors are impracticable. Even the use of deposited thin-film resistors is handicapped by the lack of available surface area on which to spread a meandered resistor pattern (see Figure 1). The meandered patterns for high-value resistor networks can occupy 0.5 square inch of surface area, a fact which does not lend itself to integrated microwatt circuit fabrication. The ability to form smaller discrete components has become a necessity, and the need to develop microminiature component techniques for use in hybrid integrated micropower circuits is thereby emphasized.

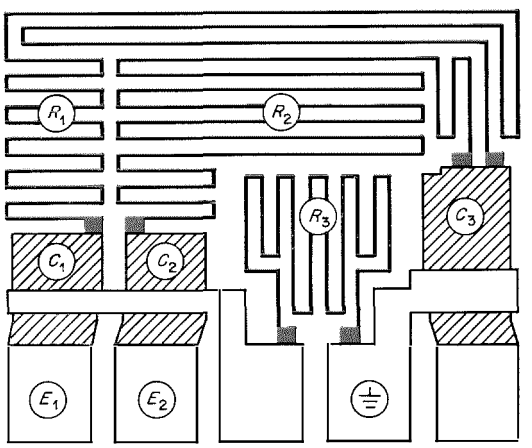

Figure 1—Meandered resistor pattern.

2. Microcomponent Considerations

Devices so tiny that medium-power microscopes are required to see their details present problems in handling, testing, and packaging. In the semiconductor industry these problems are solved by the mass production of hundreds of these devices at a time on a single slice or wafer of silicon. The process is so designed that the technician can handle these slices as if they were single entities; and when the process is complete the slices are diced or cut to separate the individual devices for mounting and packaging. Thus the cost of this somewhat expensive and elaborate process is spread to provide a low cost per device. Yield factors (the number of acceptable devices obtained per slice) are an important consideration in this operation.

Any fabrication process for microminiature resistance networks, and particularly for those networks to be produced integrally with semiconductor devices, must be designed to be compatible with batch-processing methods.

3. Planar Resistor Structure

The standard resistor employed in the thin-film circuit processes is made with the planar structure illustrated in Figure 2, where ρ is the volume resistivity of the film material, and l is the length, w the width, and t the thickness of the film. Connections are usually made with a thicker layer of a highly conductive metal which forms the interconnecting circuit proper. The value of the resistor R is calculated from the above dimensions as

$$R = \rho l/wt, \text{ ohm}$$

and the film is characterized by the resistance value of a square section ($l/w = 1$) termed the film resistivity R', where

$$R' = \rho/t, \text{ ohm per square.}$$

For a given set of geometric dimensions the resistance value can be determined by multiplying the film resistivity by the aspect ratio $a = l/w$. This resistance can be changed by changing the thickness of the film. In actual practice, limitations occur for both the thickness and lateral dimension factors as shown in Figure 3.

Standard thin-film resistors are usually made by depositing a metal such as tantalum, titanium, chromium, or nickel-chromium alloy, in a film so thin that an appreciable resistance can be obtained between the terminal connections. Since the volume resistivity of these metals is of the order of 10^{-4} to 10^{-5} ohm-centimeter as shown in Figure 4, the thickness dimension must be made very small to achieve any useful value of film resistance. The thickness commonly used is between 100 and 500 angstroms (1 angstrom = 10^{-8} centimeter).

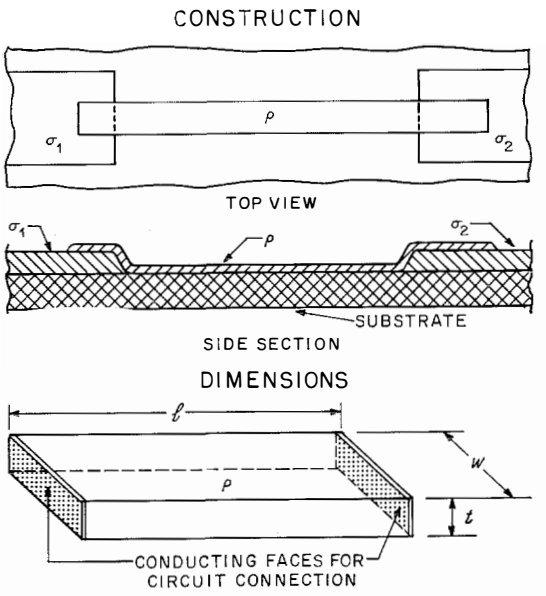

Figure 2—Planar resistor structure.

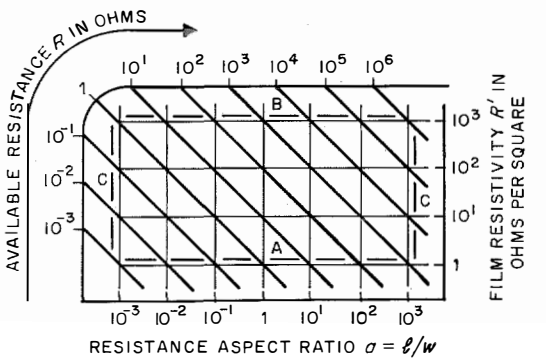

Figure 3—Limit of film-type resistance due to: *A*—contacts, *B*—stability, and *C*—geometry.

Several limitations exist on the minimum film thickness that can be used. The long-term stability is affected by the proportion of the conducting film that is converted to the nonconducting oxide which eventually grows on the film surface. Even encapsulation under a second, protective film does not completely eliminate this activity, as shown in Figure 5. The drawings of Figure 6 illustrate the amount of change to be expected from an oxide that converts a 50-angstrom layer of the film. Obviously the thinner film is less stable than the thicker film. This applies only to pure metallic films; it does not apply to cermet (ceramic-metal) mixtures which are relatively thick and conducting compounds which do not oxidize.

The available, or useable, resistivity of a particular metal film is usually determined by the value at which the film conductance crosses

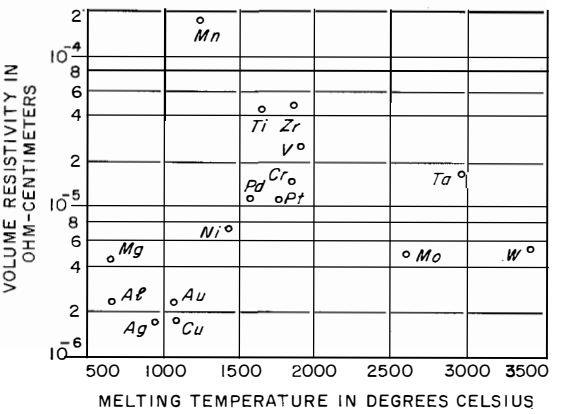

Figure 4—Resistivities of applicable metals.

from a negative temperature coefficient (semiconducting at ultra-thinness) to a positive temperature coefficient (metallic conduction). Figure 7 illustrates this effect for several materials. It is evident why nichrome films are deposited with a film resistivity near 250 ohms per square and titanium films are employed at 1300 ohms per square. Monolithic diffused resistors have film resistivities between 100 and 300 ohms per square [4]. Refer to Table 1.

Besides the factor of temperature coefficient, the resistivity of ultra-thin films also begins to deviate from the volume resistivity found in thicker sections. This deviation is presented in Figure 8 on a normalized chart [5]. The seriousness of this effect becomes apparent when it is realized that the mean free path of conduction electrons in metal is between 200 and 600 angstroms [6, 7].

Because of the limitations imposed by the above factors, metallic film resistivities range between 10 and 1500 ohms per square unless some special considerations are involved. As a result

TABLE 1
RESISTOR PROPERTIES

Property	Diffused	Thin-Film
Film resistivity R′ in ohms per square	2.5 to 300	10 to 2000
Temperature coefficient of resistivity in parts per million per degree Celsius	+500 to −2000	+200 to −400
Maximum power dissipation in milliwatts per square centimeter	100 to 250	100 to 500
Fabrication tolerance in percent	±5 to ±20	±1 to ±10
Range of values in ohms	10 to 30 000	5 to 100 000

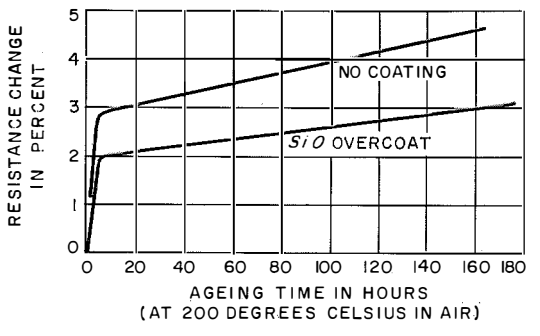

Figure 5—Ageing effect on a thin-film nickel-chromium resistor.

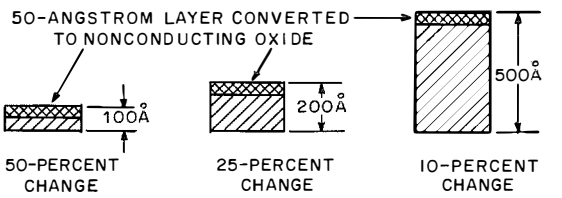

Figure 6—Surface oxidation effects on stability.

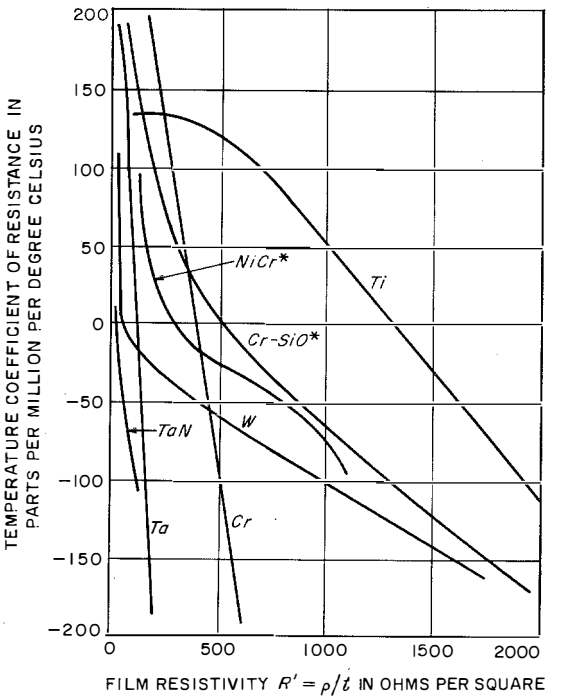

Figure 7—Dependence of temperature coefficient of resistance on thickness. The asterisks indicate high dependence on the composition ratio.

the aspect ratio (ratio of length to width) of resistors in the high values becomes large, and the area covered by the resistor is large. Figure 9 presents a nomograph for computing the area covered by a resistor of a given value R by a film of a given resistivity R' having a given width w. The aspect ratio a is also indicated. This graph does not account for the space used to separate the paths of a meandered resistor. The area of an average microcircuit (50 mils $\times$ 60 mils) is 3×10^{-3} square inch (2×10^{-2} square centimeter).

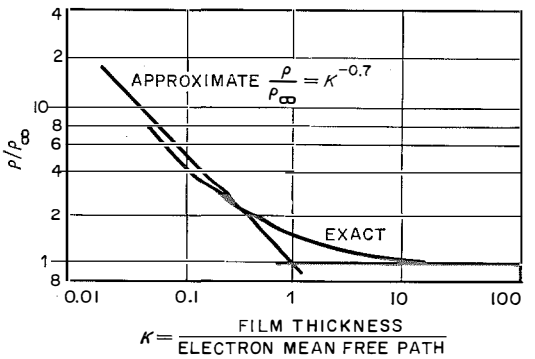

Figure 8—Effects of ultra-thinness on resistivity.

To produce resistor values in the range of 100 000 ohms requires a resistor pattern that is long, narrow, and thin. To obtain sufficient length it is necessary to meander the resistor pattern, a practice illustrated in Figure 1.

To escape from these limitations of thin metallic films, the industry has been investigating the use of cermets. Table 2 lists several of these mixtures. Thick cermet films are produced by screening formulations of mixed powders of

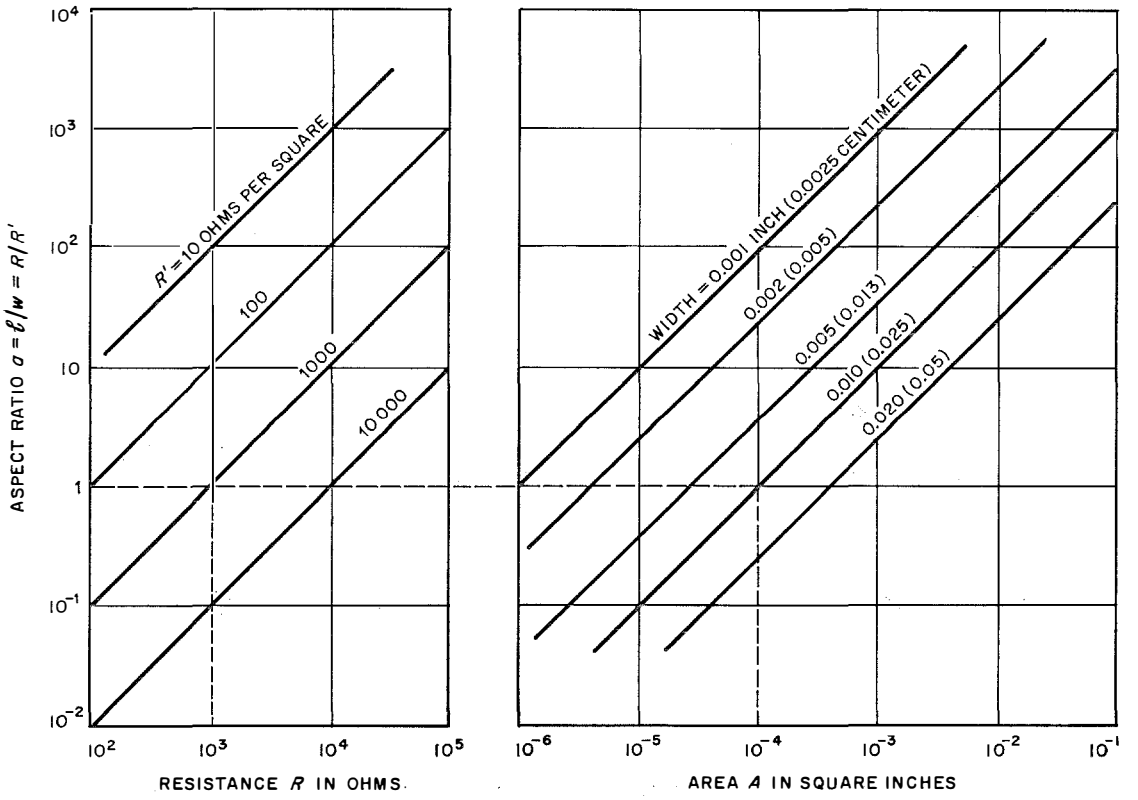

Figure 9—Area required by planar resistors. $a = R/R'$, and $A = aw^2$.

TABLE 2
RESISTIVE CERMET MIXTURES

Mixture	Resistivity* (ohm-centimeters)	Film Deposition Method	Pattern Formation Method
Pt-glass	10^{-5} to 10^{-1}	Silk-screened and fired	Silk-screening
Sn-SnO_2 (SnO_x)	10^{-4} to 10^{-3}	Pyrolytic decomposition	Kodak Photo-Resist (KPR) and etching
C-glass	10^{-4} to 10^{-2}	Silk-screened and fired	Silk-screening
Cr-SiO	10^{-5} to 10^{3}	Simultaneous or co-evaporation in vacuum	Evaporation mask or etching
Al-Al_2O_3	10^{-5} to 10^{4}	Co-evaporation in vacuum	Evaporation mask or etching
Ti-TiO_2 (TiO_x)	10^{-4} to 10^{-3}	Pyrolytic decomposition	Kodak Photo-Resist and etching
Ta-Al_2O_3	10^{-4} to 10^{6}	Co-evaporation	Evaporation mask

* In all cases, the resistivity depends on the proportions of the constituents.

conducting and insulating materials onto the substrate, and then firing these patterns at temperatures above 600 degrees Celsius. The noble metals, such as platinum and palladium, are favorite choices for conductive material, and low-temperature glasses are normally used for the ceramic [8, 9, 10]. After firing, the film consists of the glassy matrix interlaced between microscopic globules of the metallic component. Silk-screening has proved acceptable for subminiature circuit fabrication, but this method does not provide the resolution required for microcircuit deposition.

Pyrolytic deposition, which is a chemical reaction obtained at elevated temperatures, has been used for some time [11]. Where the reaction product (for example tin oxide) is etchable, fine resolution patterns can be obtained. However, usually this method is also a thick-film process, and thus suffers the same resolution limitations as the silk-screen method.

Vacuum-evaporated cermets are beginning to be used more as better methods of controlling the deposition process are developed. These mixtures can be deposited in almost any proportion, and the resistivities range from metallic to insulating. Deposition can be done either by simultaneous evaporation from two separately heated sources, or by co-evaporation from a single heated source. For compatible constituents the co-evaporation method is more easily controlled than the simultaneous method. Since these materials can be deposited as thin films, their use in microcircuit production is very desirable.

4. Sandwich Resistor Structure

To overcome the several shortcomings and limitations of the planar resistor, the feasibility of a sandwich-type resistor is being investigated [12].

The arrangement of the sandwich resistance takes the form shown in Figure 10, where again t is the film thickness, and l and w are the length and width of the electrode overlap. The product lw is the resistance area A. This geometry is contrasted with the usual planar resistor of Figure 2.

The resistance of a sandwich resistor is related to the geometry and resistivity ρ as

$$R = \rho t/lw, \text{ ohm}$$

and for a fixed area and resistivity the resistance varies during deposition as

$$R = (\rho/A)t$$

where t is the independent variable. This relationship of resistance to thickness is the reverse of that occurring with the planar structure.

Since for a given thickness the resistance varies inversely as the area, the resistor can be characterized by its unit area conductance G'' such

that

$$G'' = 1/\rho t, \text{ mho per square micron}$$

and the total resistance can be found by

$$R = 1/G''A = 1/G$$

where $G = G''A$ is the total conductance of the sandwich resistor. This parameter would be useful if the resistivity and the thickness were fixed by other considerations.

The capacitance of the sandwich resistor is much greater than that inherent with the planar structure and is given by

$$C = \epsilon A/t$$

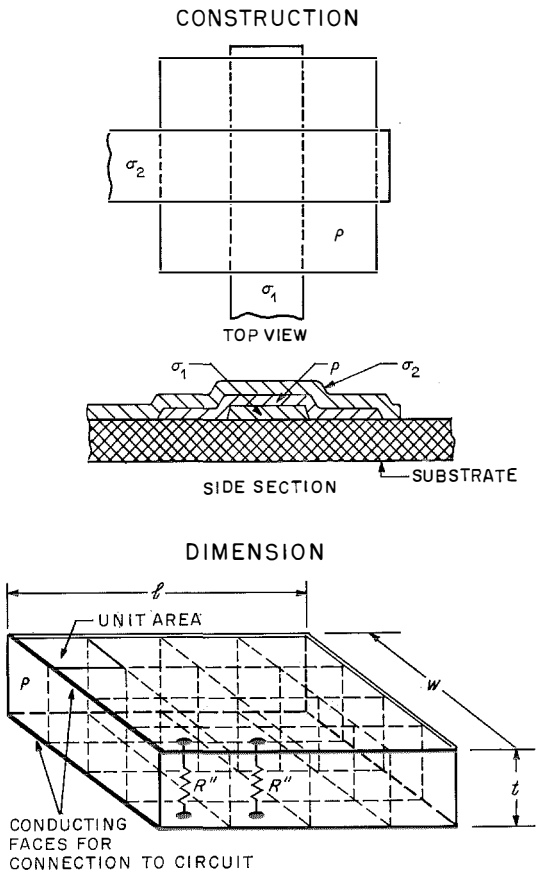

Figure 10—Sandwich resistor structure.

$$R = \rho t/lw$$
$$R'' = \rho t$$
$$R = R''/A$$
$$A = lw$$

where $A = lw$.

The resistance-capacitance product is a constant that depends only on the property of the film material and is called the dielectric relaxation time τ.

$$RC = \rho\epsilon = \tau$$

and for a given resistance the capacitance can be determined promptly for any material for which τ is known.

It is impossible to directly measure the value of a sandwich resistor during deposition because the covering electrode is not present. Thus other means of resistor value determination must be employed to control the deposition process. The resistivity of a film can be measured directly during deposition, and this value —if the volume resistivity is known—can be related to the unit conductance. However, the actual resistivity of a deposited film is often not known with sufficient accuracy to permit this calculation. For sandwich resistors the resistivity is an important factor for determining the required thickness to obtain the desired resistance value with a given electrode geometry.

It is possible to determine the resistivity of a film instantaneously (providing it is homogeneous) by measuring the volume resistivity and the thickness using present monitoring methods. The resistivity can be found directly by

$$\rho = R't$$

with the use of an analog multiplier. The unit conductance is then found to be

$$G'' = 1/\rho t$$

which also requires a multiplier. The resistance value is determined as

$$R = \rho t/A$$
$$= 1/G''A$$

where the area can be predetermined from the known electrode geometry. The required unit area conductance can be established before deposition.

The maximum area required for the sandwich structure is that area represented by the cross-over of the two lines. These lines can be as narrow as 12 microns (0.0005 inch) and they present minimum areas of 3×10^{-7} square inch (2×10^{-6} square centimeter).

The construction of the sandwich resistor is similar to the standard thin-film capacitor. The high-resistivity material is deposited between two overlapping thin-film conductors, the resistance is developed within the area of the overlap, and the result is a parallel resistor-capacitor network such as in Figure 11*A*. Since this capacitance is in parallel rather than to a ground plane as in both planar and diffused resistor structures, it can be used as a speed-up capacitance in some applications.

Several advantages are realized by the use of the sandwich structure instead of the planar structure.

(A) Because of the area dependence, the higher-value resistors take up less area than would otherwise be required.

(B) The electrodes offer a form of self-encapsulation which provides stability and protection.

(C) The use of thick films reduces the effect of surface contamination.

(D) The bulk properties of the resistance material would be used, eliminating the problem of the anomalous thin-film resistance effect.

(E) The resistance film can be deposited as a general area and the several electrode contacts can use portions of the area as needed.

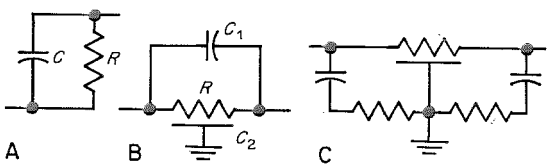

Figure 11—Resistor equivalents. *A* = sandwich resistor, *B* = planar resistor over semiconducting substrate, and *C* = monolithic diffused resistor.

To use this concept of a sandwich resistor, it is necessary to further develop the technology of employing semi-insulating compounds. Some appropriate materials are considered in the next section.

5. High-Resistance Material

There are several high-resistance semiconducting compounds which may be applicable for the sandwich resistor. Table 3 lists some of the materials presently being investigated.

A typical high-resistance material is "intrinsic" silicon which can provide resistivity values in the range of 150 ohm-centimeters in evaporated films. Using this resistivity for example, a typical set of values becomes:

Resistivity ρ	= 150 ohm-centimeters
Thickness t	= 1000 angstroms = 0.1 micron = 10^{-5} centimeter
Film resistivity R'	= 15 megohms per square
Unit area resistance R″	= 1.5×10^5 ohm-square-microns
Resistor area A	= 25 microns × 25 microns = 625 square microns
Resistor value R	= 240 ohms

TABLE 3

HIGH-RESISTIVITY COMPOUNDS

Material	Melting Point (degrees Celsius)	Evaporation* (degrees Celsius)	Volume Resistivity ρ (ohm-centimeter)	ϵ
Si	1410	1550	100	12
Ge	960	1310	200	16
SiO	1700	1050		5.5
MgF_2	395	1350		6.5
CuI	605	700	10	
CeS_2	2250	2100		
In_2S_3	1050	1100		
MoS_2	1185	1500		
CdTe	1041	750		
CeF_3	1324	1350		50 to 100

* Approximate evaporation temperature at 10^{-5} torr.

This resistance value is quite low for the general application of the sandwich resistor in microwatt circuits, indicating that silicon has too low a resistivity for general use. However, silicon has promise for a specific application now being developed. Ideal resistivities to produce large-value resistors would lie in the vicinity of 10^4 ohm-centimeters.

Work is also being done on the co-evaporation of mixtures. Both the chromium-silicon monoxide (Cr-SiO) and the aluminum-alumina (Al-Al_2O_3) phases are receiving close scrutiny. The silicon monoxide and chromium are mixed together as powder in suitable proportions and placed in a quartz crucible inside a tantalum tube heater as illustrated in Figure 12. Then when the heater is brought up to a predetermined temperature and held for a period of 10 to 30 minutes, the constituents in the crucible sublime in a proportion controlled by: (A) the ratio of their respective vapor pressures at the soaking temperature, and (B) the ratio of the respective amounts in the crucible. Since the ratio of vapor pressures is somewhat constant, the soaking temperature mainly determines the deposition rate.

In the co-evaporation of aluminum (Al) and alumina (Al_2O_3), a different procedure is employed. Instead of mixing two powders as previously described, the powdered alumina is placed in an alumina crucible and a relatively large mass of aluminum is bedded into the powder. The crucible is then placed in a tube heater as before. As the assembly is heated, the aluminum melts at 660 degrees Celsius and forms a ball as shown in Figure 13. As the temperature is raised further the aluminum begins to dissolve the alumina powder with which it is in contact and maintains a continuously changing equilibrium. At a temperature near 1300 degrees Celsius a chemical reaction occurs between the aluminum and dissolved alumina. This reaction forms another compound which is stable only at this elevated temperature; it may be aluminum monoxide (AlO) or aluminum suboxide (Al_2O) [13]. This compound has a relatively high vapor pressure and evaporates from the surface of the aluminum. The vapor deposits a tough, clear, transparent, insulating film of unknown constitution. As the temperature is further increased the vapor pressure of the aluminum becomes noticeable, and both the compound and the metallic alumi-

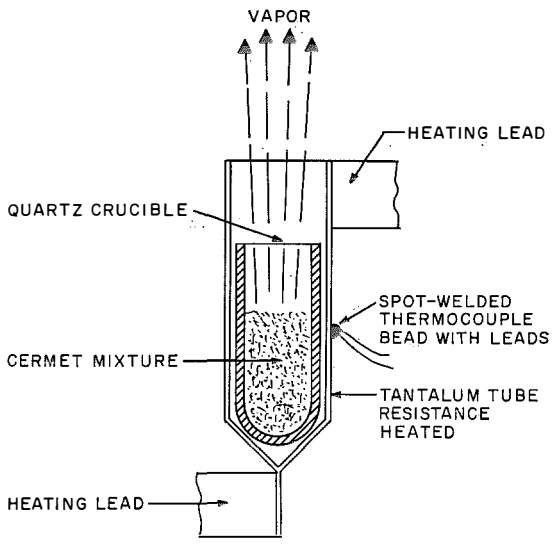

Figure 12—Cermet co-evaporation.

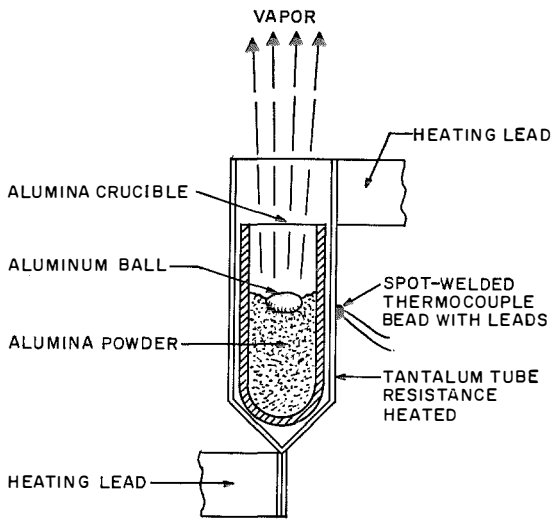

Figure 13—Aluminum-alumina co-evaporation.

num are present in the vapor. The resulting deposit is a grayish transparent film which retains its glassy appearance but can range from clear to opaque with an aluminum-like luster. The resistivity of the film also ranges from insulating to conducting.

An extensive program is in progress to tabulate the range of resistivities and the controlling variables of the process so that these two high-resistivity cermets may be used in some particular applications. The aluminum-alumina method is the most promising since the film is easily etchable to fine geometry by standard Kodak Photo-Resist procedures. (Pure alumina is not etchable and evaporates at temperatures above 2000 degrees Celsius) [14].

Other work has been done on the mixtures of co-evaporated tantalum and alumina (Ta-Al_2O_3). An alumina rod was wrapped with tantalum foil, and this tube and core were heated in an electron-bombardment-evaporator arrangement, shown in Figure 14 [15]. When the temperature at the tip of the rod approached 2000 degrees Celsius, the alumina melted. The molten alumina wets the tantalum foil, and the tantalum (which itself melts at 2900 degrees Celsius) dissolved into the molten alumina. The tip of the rod became a black glassy mass. As the heat was increased the alumina evaporated and carried some of the tantalum with it. (The vapor pressure of tantalum is quite low even at these temperatures.) The vapor deposited a grayish glassy film the optical density of which depended on the amount of tantalum dissolved in the alumina. As the alumina evaporated, the tantalum would build up a concentration in the melt, and the resistivities of the deposited films were not controllable as a result.

6. Fabrication Techniques

Since the sandwich resistor involved the overlap of very narrow electrodes, test patterns for the development program must approximate the size ultimately used to provide meaningful data for evaluation.

Using photo-reduction techniques, a 6-component matrix pattern was obtained which was then step-repeated on a master mask. For this initial test program the patterns were etched into evaporation masks, although different processes could possibly be used for later development. The complete pattern overlay is shown in Figure 15, the lines on the resistive film

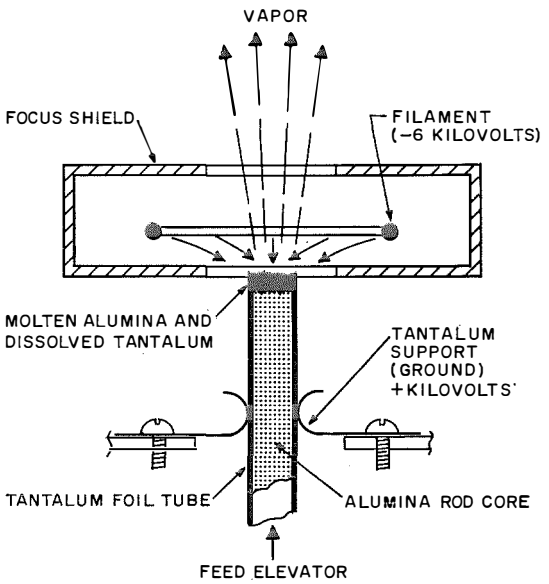

Figure 14—Electron-beam evaporator.

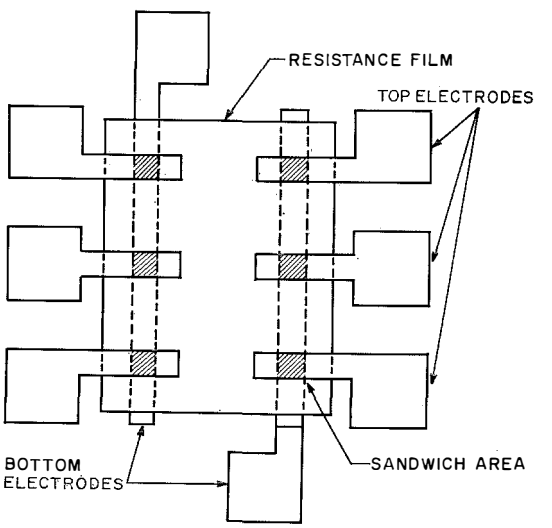

Figure 15—Resistor test pattern.

being 75 microns wide. Each crossover presents an area of 5625 square microns. The resistor film is of such high resistance that there is no appreciable connection between elements except at the crossovers.

The test patterns were deposited on silicon slices which had been polished and oxidized to provide a quartz surface (Figure 16). This substrate was used since the devices eventually will be applied on just such a surface. Borosilicate and aluminosilicate glasses were not used except for the crudest basic tests. After deposition, the silicon slice was diced and each die, containing one complete matrix, was mounted on an 8-lead transistor header. Thermocompression gold bonding was then used to connect the components to the header leads to provide connections for further testing. See Figure 17.

The computation required for the monitored deposition of a sandwich resistor is given in the diagram of Figure 18, where the blocks with the times signs are the multiplier functions. The values of R' and t are measured by external instruments and connected to the computer input. Within the computer the values of ρ and R'' are available and can be monitored separately.

Two magnetoresistance devices were employed to perform the multiplying functions. A commercial unit, the Mistor Multiplier model *MMA-3001,* was selected for this purpose. The circuit, composed of the multipliers and commercially available differential amplifiers, is presented in Figure 19. To prevent undue loading on the differential amplifiers, booster amplifiers were used between several sections. The meters indicate the values of the several internal parameters, and output jacks are provided for recording these values if desired.

An adjustable voltage-divider resistor is used to perform the division functions. A 10-turn adjustable resistor is connected in the feedback circuit of the associated differential amplifier in such a way that the amplifier gain is the reciprocal of the dial reading. The dial is calibrated between 1 (unity) and 11. This calibration provides a range between powers of 10, and the powers-of-10 factors are kept track of externally in setting up the computer calibration.

The values of R' and t are determined by two instruments in an associated deposition control system [15], and the values are given to the computer by means of patch plugs.

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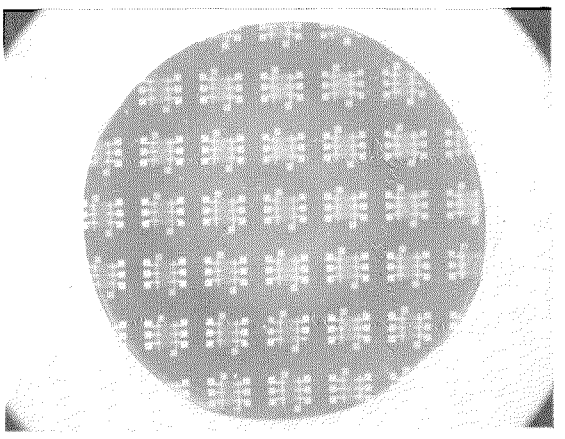

Figure 16—Test patterns deposited on quartz substrate.

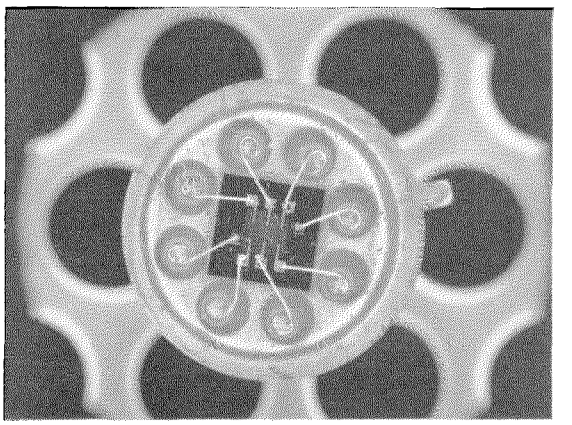

Figure 17—Matrix mounted on header with connections made.

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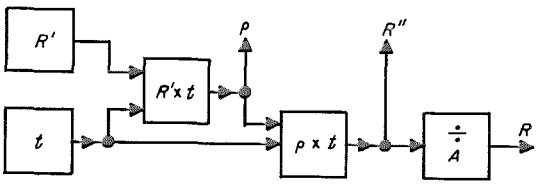

Figure 18—Computation diagram.

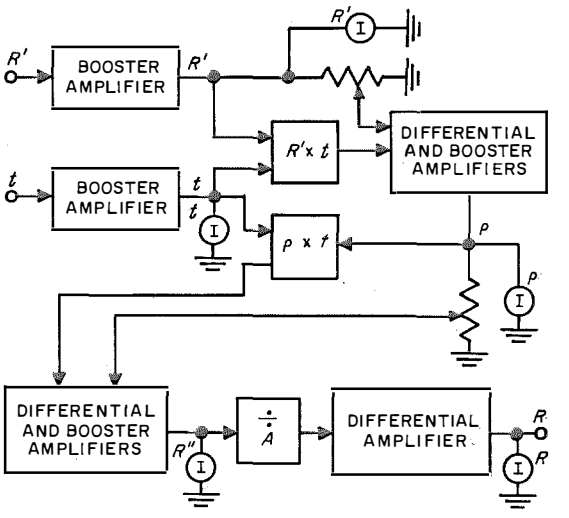

Figure 19—Analog-computer block diagram.

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Selecting Digital Integrated Semiconductor Circuits

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1. Introduction

Integrated monolithic solid-state circuits with semiconductor elements have rapidly gained importance the past few years and find increasing application in electronic equipment. The use of these circuits is justifiable if they offer improvements over conventional components. Such advantages may be increased reliability, lower cost, less weight or volume, and shorter development time. The relative weighting of the individual improvements depends on the field of application and on the type and size of the equipment in which the integrated circuits are used.

2. Microstructure

Selecting the right family of integrated circuits constitutes a multiple problem as can be demonstrated with a simple example.

Assume that integrated circuits are to be selected for a stationary digital data processing system of substantial size. The majority of circuit functions are of the same type and therefore particularly suitable for standardization. As a large number of relatively simple circuits in a narrow range of types is required, monolithic silicon integrated circuits are highly commendable for this application.

Standardized monolithic units are available commercially. Integrated circuits can also be manufactured to customers' specifications or can be produced from master slices.

The basic development cost of a new integrated circuit is of the order of DM 60 000. Therefore a careful investigation is required to reveal if this cost is justified.

In the so-called master-slice method, different circuit configurations can be realized with a single standard silicon chip by using various conductor patterns because all the diffused elements are insulated from each other. In this way, the basic cost per circuit type is low even for a relatively small quantity. This permits a compromise to be reached between the low cost of commercially standardized integrated circuits and the adaptability of very expensive circuits developed to the customer's specifications.

In the example of the electronic data processing system, special developments are virtually unnecessary and commercially available integrated circuits will be used.

3. Selecting the Family

3.1. General

The most advantageous family of integrated circuits is best selected by determining the most suitable gate circuit.

The basic circuits in our example should have a typical propagation delay of 50 to 70 nanoseconds. Their cost should be low and they should be highly immune to interference voltages. Contrariwise, their power dissipation is relatively unimportant.

Essential considerations in the evaluation of possibly suitable integrated-circuit families are the feasibility of providing the needed functions, electrical properties, tolerances, and relative cost of the integrated-circuit elements.

When integrated circuits are produced by diffusion, the cost for one resistor of 5 kilohms is the same as for one 50-picofarad capacitor, one diode, or one transistor. However, while diffused resistors and capacitors have relatively poor electrical properties and wide tolerance ranges, integrated-circuit transistors and diodes with, say, subepitaxial structure are comparable in performance with conventional components. This fact suggests the use of circuits having small numbers of resistor and capacitor elements, but favoring diodes and transistors.

Figure 1 shows the most widely used basic gate circuits, the characteristics of which are given in Table 1. Many characteristics are interdependent and subject to the circuit configuration and dimensioning, power dissipation, switching speed, maximum admissible noise voltage, and maximum output load. Therefore,

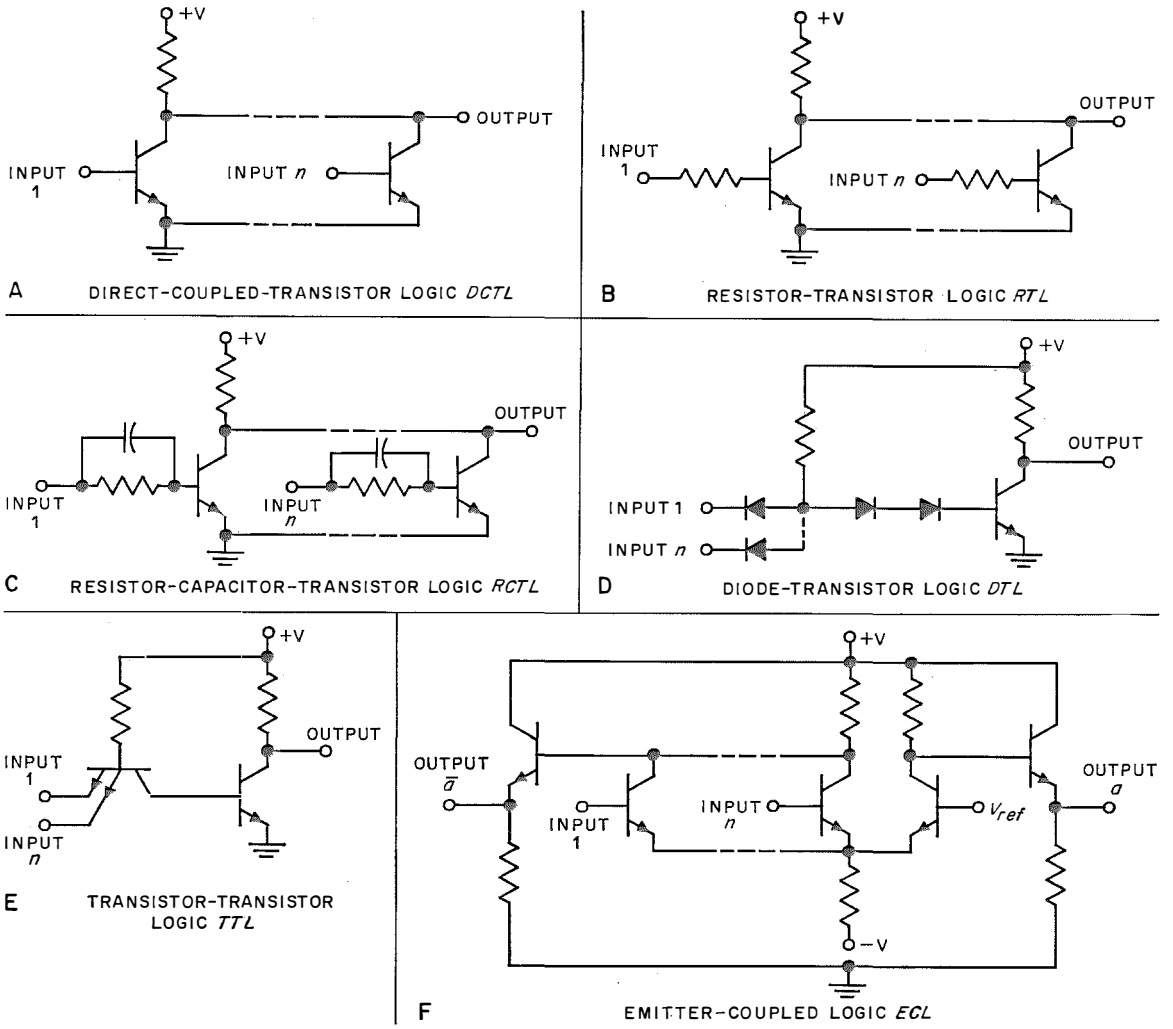

Figure 1—Basic gate circuits.

TABLE 1

TYPICAL PROPERTIES OF COMMERCIALLY AVAILABLE GATES

Type of Logic	Minimum Signal (volts)	Mean Power Dissipation (milliwatts)	Mean Delay (nanoseconds)	Maximum Permissible Noise (millivolts)
Resistor-transistor or direct-coupled-transistor *RTL, DCTL*	≈0.6	2–25	10–40	100–250
Resistor-capacitor-transistor *RCTL*	≈1	2–10	60–200	100–250
Diode-transistor *DTL*	≈1.5	5–60	8–80	300–1000
Transistor-transistor *TTL*	≈1	10–40	5–30	300–1000
Emitter-coupled *ECL*	≈0.4	10–60	2–15	80–500

improving one parameter may impair another. It has been attempted to counteract this disadvantage by providing additional active and passive elements. Figure 2 exemplifies modified diode-transistor logics. This solution, undesirable in the case of conventional components, is justifiable for diffused integrated circuits because the individual integrated circuit generally bears but a small part of the total additional cost. On the other hand, the performance is substantially improved, a reduction in the number of integrated circuits is possible, and a reduction in system cost is thus obtained.

3.2 Evaluation Viewpoints

For digital application, integrated circuits are in most cases evaluated with respect to sensitivity to noise, flexibility, power dissipation, cost, and reliability.

3.2.1 *Noise Sensitivity*

The input and output devices of our assumed data system comprise electromechanical components generating high noise voltages that are difficult to eliminate. Hence, special stress must be laid on high immunity of the integrated circuits to noise voltages, so the range of types for selection is narrowed down to transistor-transistor and diode-transistor logic.

The maximum permissible noise voltages stated in Table 1 are for direct current. The insensitivity of integrated circuits to noise pulses increases with decreasing noise pulse duration. Figure 3 shows the basic relationship between permissible noise amplitude and noise pulse duration with the integrated-circuit switching

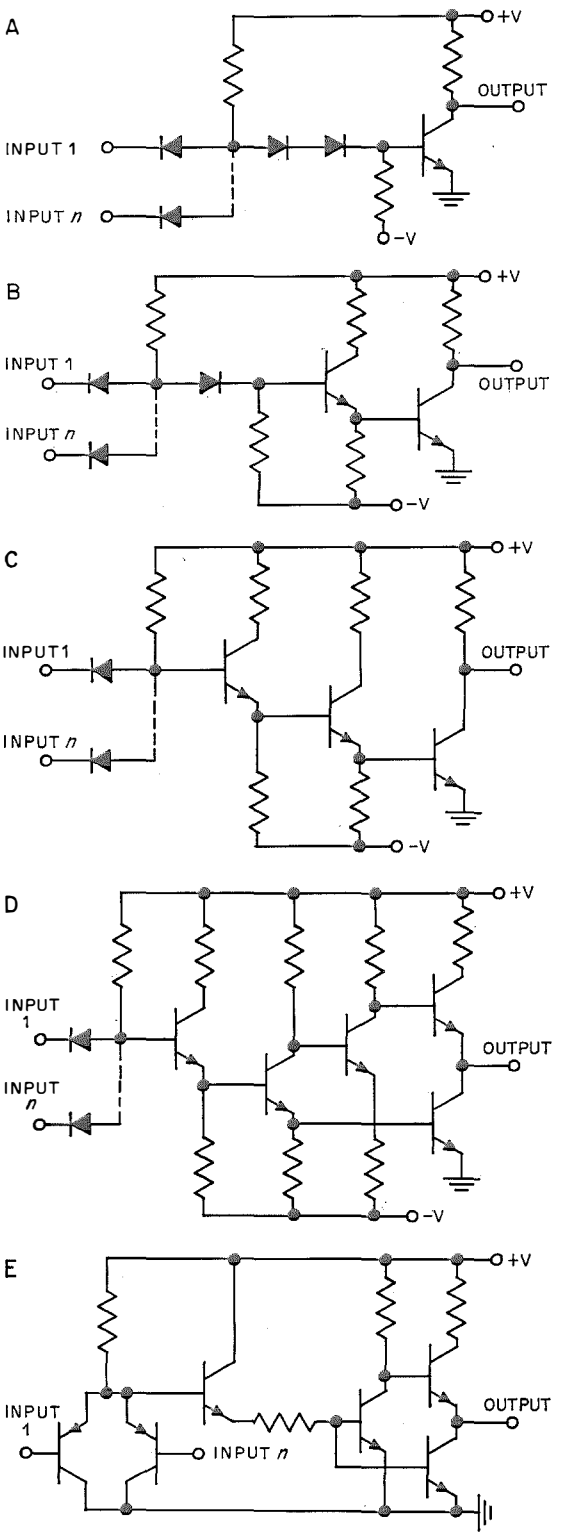

Figure 2—Modifications of diode-transistor logic. *A* is the simple diode-transistor gate. *B* increases the output current by adding an *n-p-n* transistor. *C* has two additional *n-p-n* transistors. *D* has an output amplifier. *E* reduces input current by putting a *p-n-p* transistor in the input.

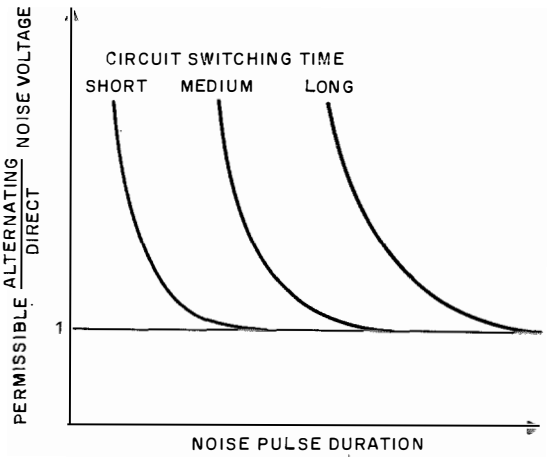

Figure 3—Permissible noise voltage amplitude plotted against noise pulse duration for short, medium, and long switching times for the integrated-circuit gate.

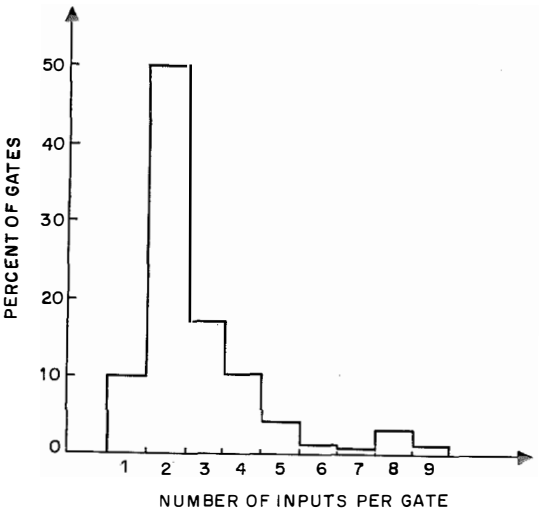

Figure 4—Number of inputs per gate in several representative data processing systems.

time as a parameter. In the interest of functional reliability of the equipment, it will be well to select only those integrated-circuit families just reliably ensuring the desired switching time in the worst case under certain ambient conditions, as faster circuits would increase the sensitivity of the equipment to noise.

For our assumed data processing system, then, the diode-transistor logic is more favorable than the transistor-transistor logic because it can be produced with greater yield due to the smaller area needed per circuit on the silicon wafer.

3.2.2. *Flexibility*

The flexibility of basic integrated circuits is of great importance for the overall cost of the equipment. Certain flip-flop circuits are most urgently needed in addition to a large number of different gate circuits. In many cases the cost can be significantly reduced if, apart from the *RS* flip-flop, a *JK* flip-flop is available that is better suited for counters and shift registers. As may be seen from Figure 4, gates with 2 or 3 inputs are rather frequently used in data processing systems. The distribution shown is the result of an investigation of 5 data processing systems of different designs and sizes; it may be assumed that this distribution is typical. Therefore it is desirable to accommodate as many 2-input or 3-input gates as possible in one common case to reduce the required number of packages for the realization of a given system function.

The flexibility is also influenced by the maximum load permissible for the integrated circuit and by the number of inputs that is often increased by so-called expanders.

It is advantageous for the system if a gate also features negation. Often integrated circuits interwork with system units that, because of high power or high signal voltage, use only conventional components. The matching circuits can be substantially simplified in some cases by the use of integrated circuits having suitable output characteristics. Large current and large voltage swings at the output of the integrated circuit are desirable.

3.2.3 *Power Dissipation*

The minimum feasible power dissipation of digital monolithic integrated circuits is provided

by the lowest possible supply voltage and the highest possible resistance. The lowest supply voltage depends on the circuit, that is, the ratings and tolerances of the integrated components. It is about 3 volts. At present the state of production methods permits resistance up to 30 kilohms. The minimum power dissipation of a monolithic gate may be of the order of 1 milliwatt when boundary conditions, such as maximum permissible noise voltage and load carrying capacity of the outputs, are observed. In practice, however, values will be higher (Table 1) because of the specification of switching time.

The feasible maximum power dissipation of an integrated circuit is determined by the rate of heat transfer from the source. At present the minimum thermal resistance in free air is 100 degrees Celsius per watt for flat packs and dual in-line packages. This corresponds to a maximum dissipated power of 0.5 watt at 125 degrees Celsius junction temperature and 75 degrees Celsius ambient temperature.

In the example chosen, enough space is assumed for the integrated circuit so that no heat problem is encountered. The power dissipation of the integrated circuit can be disregarded in this case.

3.2.4 *Cost*

In the production of integrated circuits, many hundreds of circuit elements are provided in several successive diffusion operations. The cost of material can be neglected in comparison with the cost for photomasking and processing of the silicon chips. Thus, the cost of an integrated circuit depends greatly on the quantity made, on the area per circuit, and on the yield. The area needed for a circuit is determined by the resolution in the photographic process, the type and number of circuit elements, and the number and size of insulating junctions.

The prices for mounting cases are still relatively high compared with the cost of the integrated circuit itself. The outline and design of the case therefore control to a large extent the price of the circuit. Very favorable are the prices of *TO5* cans having up to 12 terminals in most cases. Flat packages with more terminals and various outlines are much more expensive, but economize on space. The terminals are mostly on 0.05-inch (1.3-millimeter) centers. For this reason, welding of connecting strips to special, relatively expensive, wiring boards is required in place of dip soldering.

Lately low-cost dual in-line packages with integrated circuits have become available. They combine the advantageous shape of the flat packs with the possibility of mounting by dip soldering.

For cost considerations, the dual in-line package was chosen for the example of diode-transistor-logic circuits discussed here.

Many integrated-circuit families are supplied for different temperature ranges, such as +15 to +55, 0 to +75, or −55 to +125 degrees Celsius. They are all produced in one manufacturing series and differ only in testing. For the maximum temperature range, the guaranteed ratings are tested to the extreme limits stated. For the narrower ranges, the guaranteed ratings are normalized to 25 degrees Celsius and tested at only that temperature. The narrower ranges can therefore be sold at lower prices. For the data processing system under consideration, the medium temperature range from 0 to +75 degrees Celsius was chosen.

The prices for integrated circuits have not yet reached their final level and will continue to decrease, thus resulting in less expensive or more effective equipment. Figure 5 shows the mean price development to be expected for a case containing 3 diode-transistor-logic circuits.

3.2.5 *Reliability*

The production methods for integrated circuits have been modified and improved frequently. Therefore it is extremely difficult to obtain

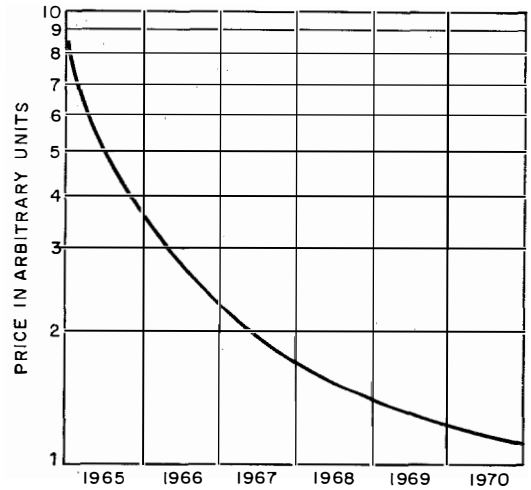

Figure 5—Expected relative price development for monolithic diode-transistor-logic gates.

data on reliability. Several component manufacturers in the United States have made extensive life tests. The results now available are based on about 100-million circuit hours. The rate of catastrophic failures amounted to about 0.001 percent per 1000 hours with a confidence level of 60 percent. This value compares well with that of best-grade silicon planar transistors.

The reliability thus attained dictates that we must not disregard the failure rates of associated equipment. The failure rate of a soldered joint is 0.0001 percent per 1000 hours, which means that this joint is only one order of magnitude more reliable than the complete integrated circuit.

The reliabilty of equipment can therefore be considerably increased when conventional components are replaced by integrated circuits. This increase stems from the low failure rate of integrated circuits and the drastic reduction in external connections.

3.3 Result and Forecast

The selection of the proper integrated-circuit type depends on the problem and on the time this selection was made. Time is significant because further development of the technology will produce new solutions. After all viewpoints had been considered, the diode-transistor logic was selected as the most suitable for the case in hand. In an actual case, three diode-transistor-logic families from different manufacturers were selected along the lines evolved in the example. Paying due attention to certain limitations, the circuits of these three families could be combined.

Modifications and improvements in future manufacture will increase the reliability and will result in integrated circuits having more than 1000 circuit-element functions, thus replacing a number of equipment units. This will have far-reaching effects on equipment and system concepts and will cause further price reductions for the complete systems.

Adolf Weygang was born in Heidenheim, Germany, on 6 March 1933. He studied telecommunications at the Staatliche Ingenieurschule in Esslingen.

In 1954 he joined Standard Elektrik Lorenz as a laboratory engineer studying components. Since 1955 he has worked on the development of electronic basic circuits. In 1959 he was appointed chief of the laboratory for basic circuits.

Noise Considerations in Microelectronic Digital Computers

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1. Introduction

The *ITT 9100* was designed to fill a need for an inexpensive and reliable store-and-forward communications computer. A complete 16-line switching center is shown in Figure 1 and a simplified block diagram of the system is shown in Figure 2. The basic clock frequency is 2 megahertz and the typical logic gate switching time is 20 nanoseconds.

Microelectronic construction was chosen for reasons of cost and reliability. Design studies repeatedly showed a 2:1 cost advantage over circuits assembled from conventional components. At present, this cost advantage applies when using commercial-grade microelectronic packages for use in an ambient of 0 to +65 degrees Celsius. The forecast sevenfold increase in system reliability is being confirmed, as the prototype has now operated 2000 hours without a failure.

The same criteria must be applied to microelectronic circuits as to conventional components; that is, speed, power consumption, reliability, noise rejection, cost, adaptability to the problem at hand, et cetera.

Construction details of the *9100* are briefly stated to provide a frame of reference. Packaging used *TO5* cans mounted on a single-layer printed-circuit board, 7 inches (180 millimeters) high and 9 inches (230 millimeters) deep. The board can accommodate a maximum of 25 cans. Etched wiring is used on both sides of the board. *TO5* cans were chosen for ease of handling and because they may be easily flow soldered. Flat packs usually require welding and the newer dual in-line pack was not then available. The circuit boards are mounted in

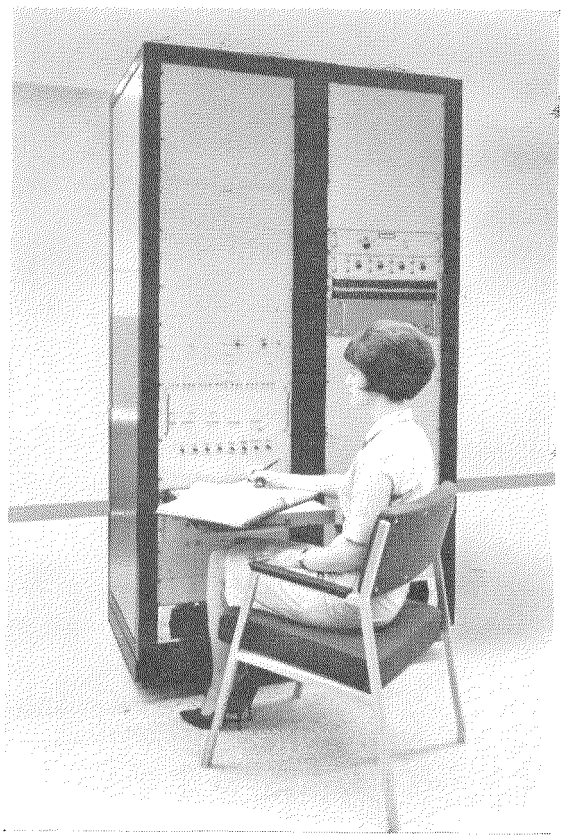

Figure 1—Complete 16-line switching center.

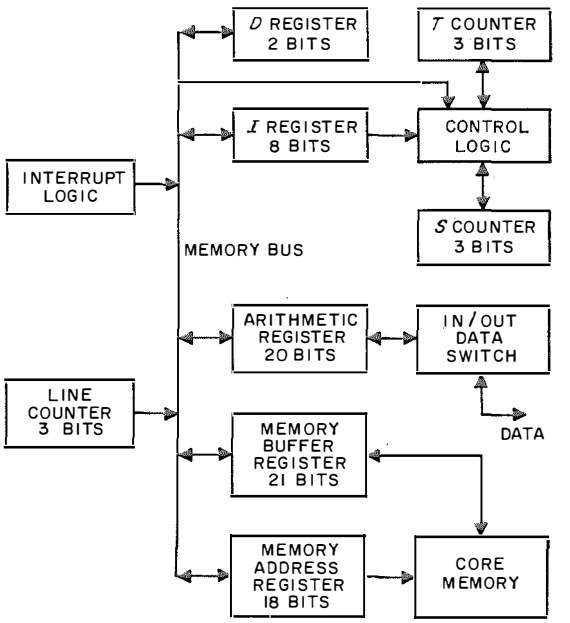

Figure 2—Functional diagram of *ITT 9100* communications computer.

nests holding 20 cards. A card-side view of the processor is shown in Figure 3.

The circuit constraints occasioned by the nature of a digital computer are described in Section 2 and a detailed discussion of system noise is given in Section 3.

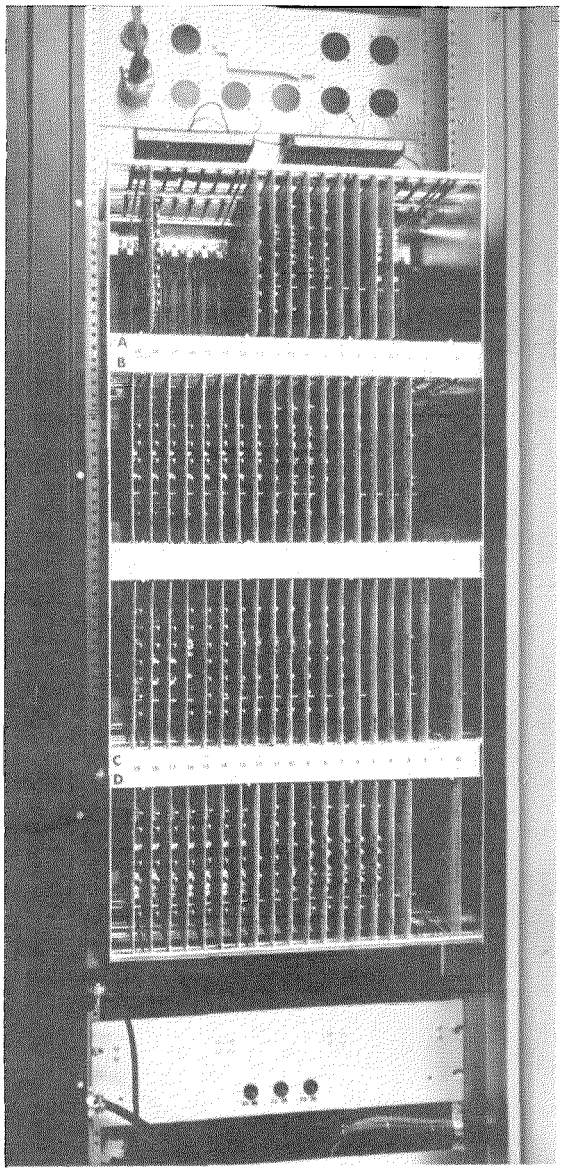

Figure 3—View of processor showing printed-circuit boards on which *TO5* cans are mounted.

2. Circuit Constraints of Stored-Program Digital Computers

There are certain characteristics of a stored-program computer that should be briefly discussed for the sake of clarity of the succeeding material. A digital computer makes use of large numbers of modules; therefore, anything that affects the piece-part cost, the assembly cost, the documentation, test, design time, power consumption, and so forth, is repeated many times and can significantly affect final cost and performance.

Heretofore, most of the computers built from integrated circuits have been small, wired-logic machines, running on fixed routines. There is a considerable difference between stored-logic and wired-logic machines. With stored-program machines, the program itself is completely unknown to the hardware designer, who has no means of predicting what sequences of instructions and patterns of data may occur in the field. A wired-logic machine, on the other hand, operates with fixed routines where the instruction sequence is more predictable. Testing is simpler and, should certain areas cause trouble because of noise pickup, the wiring can be rerouted and become part of the design. This becomes impractical in a stored-program machine, which must be prepared for all possible combinations of signal patterns and must provide adequate performance margins without making the design so conservative as to be overly expensive.

The bulk of the logic of a stored-program synchronous computer is of the form shown in Figure 4.

Flip-flop *A* is set (or reset) at clock time, the new logic state propagates through a chain of

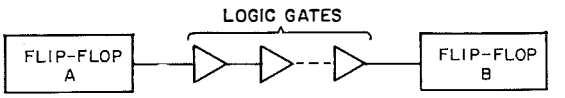

Figure 4—The type of logic most frequently used in a stored-program synchronous computer.

logic gates, and flip-flop B is set at the next clock time. The chain of gates may become quite long, often reaching 10 to 15 gates in series. Despite the tendency to think of a logic gate as a switch, it is also an amplifier with a threshold against noise on each end of the input characteristic. We now have a long cascade of amplifiers, so that if anywhere in the chain an unwanted signal exceeds the noise threshold by only enough to make the net gate gain slightly greater than 1.0, the signal has escaped control and may well be amplified to a full-valued logic signal when it reaches the receiving flip-flop. The net gate gain is that which includes the effect of the noise threshold, that is, a gain that would give a 1-volt output for a 1-volt input.

A good deal of noise can be tolerated as long as a flip-flop is not set erroneously, and therein lies one of the chief advantages of a synchronous system. It is not the noise in the gates, per se, that we care about, but the effects on the flip-flop. Since the flip-flop is a memory element it will retain the erroneous information even after the noise signal has died away. This almost always causes a machine error. The same reasoning applies to other devices, such as core memories, where a good deal of noise can be tolerated as long as a core is not switched erroneously.

3. Noise in Digital Systems

One of the most frustrating yet challenging areas of digital computer design is the question of noise. The term noise, as used here, is neither the classical white noise nor the thermal noise generated within the transistor itself; it is a broader concept to cover all departures of waveform from the ideal. These departures are caused by a number of factors, each of which is discussed below. The reason for the frustration is that the noise performance of a new system is the most difficult thing about it to predict. Direct-current loading, limiting wire lengths (from a reflection standpoint), switching speed, and capacitance loading all may be estimated in advance with reasonable accuracy. However, due to the lack of even good approximations for estimating system noise, the designer is left in a wide area between an overly conservative (and expensive) design and a system with large amounts of random noise.

3.1 Classifications of Digital System Noise

There are six general types of noise in a digital computer.

(A) Radiated and conducted from sources outside the computer.

(B) Junction notches.

(C) Reflections from unterminated lines.

(D) Common power-supply coupling.

(E) Reactive coupling between computer circuits.

(F) Common ground-impedance coupling.

The first type of noise is controlled by shielding and by filtering of power input lines. Usually a simple power line filter and steel cabinets are sufficient. Additional internal shielding is usually not required unless many devices such as relays are used and conventional suppression of contact arc is insufficient. A detailed discussion of this type of noise is beyond the scope of this paper but if such noise is present, it will usually appear as sharp spikes and the ability of the circuits to reject it will be directly related to the noise rejection discussed for types **(D)**, **(E)**, and **(F)**.

Junction notches are caused by imperfect balancing of charges or by the finite turn-on and turn-off times of semiconductor junctions in both diodes and transistors. This type of noise is usually of the order of 0.25 to 0.5 volt, but is rarely serious because it occurs at times when it can be tolerated, and also is usually of a polarity that does not hinder circuit operation. Reference to it is included only for completeness.

The third type (reflections from unterminated lines) is quite common and is the major factor limiting the length of wire that may be attached to a gate. With rise times of 20 nanoseconds there will be a significant amount of energy at 17.5 megahertz, and at this frequency a line 2 feet (0.61 meter) long has an electrical length of 12 degrees. This length is sufficient to introduce a noticeable reactive component. Wires longer than this rapidly become cases requiring termination through the use of expensive low-impedance drivers. The parallel nature of a high-speed computer requires a large number of signal paths. Even assuming inexpensive drivers, the power consumed in the terminations would become a heavy burden.

Since reflection noise is directly related to the switching speed and the voltage excursion, the degree of problem encountered with a given circuit will be a function of the slope of the waveform, or dv/dt, which takes into account both the voltage swing and the speed. Use of dv/dt as a comparison is discussed further in a subsequent paragraph. This type of noise also includes inductive ringing of an insufficiently damped line.

A distinction should be made here between harmful and harmless reflections. If positive logic is assumed and the logic changes from *1* to *0*, this negative transition is propagated down the line. With the usual case of the terminating resistance being higher than the line impedance, the negative transition will be reflected in phase. This adds to the *0*, actually aiding the turnoff of the next stage. When this negative spike, however, reaches the driver, which usually has an impedance of less than the line, the negative spike will be reflected as a positive spike and may well be large enough to overcome the noise threshold of the driven gate.

This positive backswing is one of the two major limitations on wire length. The other was the negative backswing on the positive-going transition. Another distinction between harmless and harmful noise can depend on system timing. There are cases where crosstalk occurs only at a time when clock pulses do not exist and the transient dies away before the next clock pulse.

The fourth type of noise (common power-supply coupling) is caused by the inability of the power system to respond to rapid demands for current. The voltage on the power bus changes and this change is coupled to other circuits on the same line. If the voltage change is in opposition to the signal being propagated by a second circuit, errors may result. This type of noise is a function of both the magnitude and speed of the current required by a switch, and the ratio di/dt encompasses them both. The use of this ratio is also discussed below. This type of noise is also the easiest of the four major types to cure since proper filtering is relatively easy to achieve.

The next major type of noise is brought about by direct reactance coupling from one logic circuit to another. Jarvis [1] has made a theoretical analysis of noise coupled from one etched line to another and verified the predictions with experimental results. His analysis is limited, however, to the case of lines terminated at both ends in their characteristic impedance and in the presence of an underlying ground plane. When the lines are not terminated, he indicates that an approximation can be made that will be off by no more than a factor of *2*. Since the system noise levels often are greater than half the available noise rejection, a better approximation could be wished for.

Actually, the major obstacle to accurate noise prediction is the tremendously complicated task of analyzing the length and proximity of the backplane wires under all possible signal conditions. Figure 5 shows the backplane wiring and memory cables of the *9100* prototype. Most of these wires carry signals with 20-nanosecond rise times. The capacitance coupling from one circuit to another is a direct function of both excursion and rise time, or again, dv/dt, and the inductance coupling is a function of di/dt. Logic circuits with large voltage

swings generate more noise of this type than circuits with small swings, the rise and fall times being equal. This type of noise can be controlled by shielding; however, the speed of modern computers and the thousands of interconnections raise the economic problems of manufacture and the electrical problems of performance. Excessive shielding introduces extra capacitance to ground, thereby affecting the speed of operation.

It is also of interest that there is more coupling between two etched lines on a printed-circuit board than might appear at first glance. Two parallel printed lines, each 0.030 inch (0.8 millimeter) wide with a separation between inside edges of 0.066 inch (1.7 millimeters) etched in copper sheet 0.0028 inch (0.07 millimeter) thick (2-ounce copper), mounted on a glass epoxy board with a dielectric constant of 4.0, exhibit a mutual capacitance of approximately 0.9 picofarad per inch (0.035 picofarad per millimeter). Two such lines running the 7-inch (180-millimeter) length of the *9100* mother board have a mutual capacitance of approximately 6.3 picofarads. The mutual inductance between these etched lines is approximately 0.141 microhenry. A simplified model of the coupling mechanism is shown in Figure 6A, and the response of the receiving line is shown in Figure 6B.

Treating the parallel lines as a lumped circuit, it is possible to examine the inductance and capacitance components of coupling separately. This approximation is valid largely because the propagation time from one end of the etch to the other is less than 1 nanosecond and the transition time used here is 20 nanoseconds. The potential along the sending line is therefore very nearly uniform with respect to time. If the signal on the sending line is a 6-volt 30-milliampere transition occurring in 20 nanoseconds and Z_L is 1000 ohms, a 1.5-volt spike will be coupled due to the capacitance and another

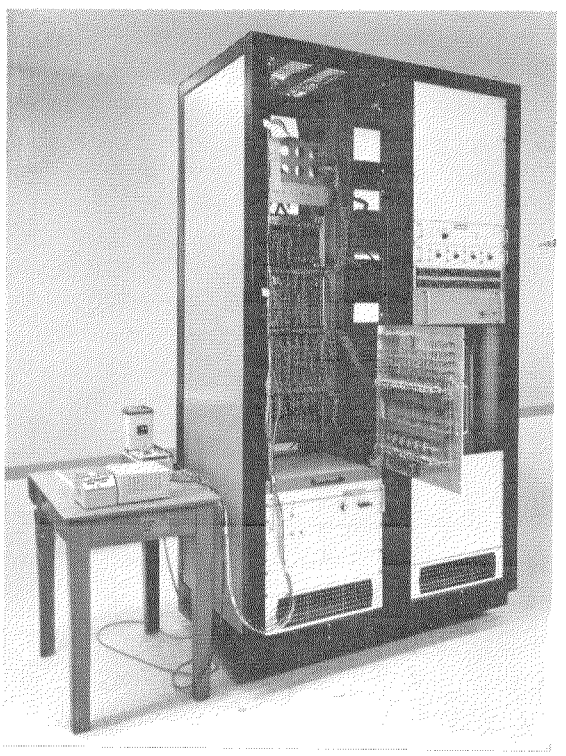

Figure 5—Back-plane wiring of prototype computer.

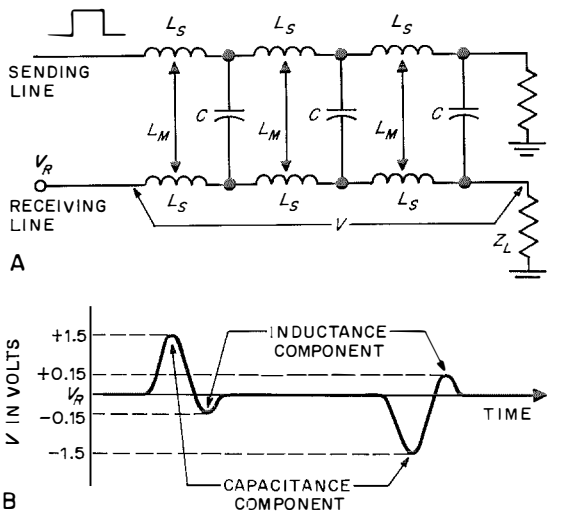

Figure 6—*A* is a simplified model of the coupling mechanism between two parallel lines on a printed-circuit board and *B* is the response in one line to a square wave in the other line. V_R is the nominal voltage of the receiving line, either 0 or + 5 volts depending on the state of the signal.

spike of 0.15 volt is due to the inductance coupling. These two spikes can be seen in Figure 6B. The transient spikes are shown centered about V_R, the nominal voltage of the receiving line, approximately 0 volts or +5 volts depending on the logic state of the gate driving the receiving line. Since the receiving line is relatively short, the spikes appear in essentially the same form at both ends of the line simultaneously.

The lumped circuit simplification becomes less valid as the length of the parallel lines increases. The experimental results for etches 2 or 3 times as long as this example are less easily explained and further work remains to be done. In the *9100* board, the inductance effect is an order of a magnitude less than the capacitance effect, at least on lines of 7 inches (180 millimeters) or less. In the longer lines, the self-inductance of the receiving line apparently rings because of the excitation of the capacitance-coupled energy.

The capacitance between etched lines may best be estimated by means of a field map, readily yielding results to ± 10 percent and avoiding the involved mathematics of a precise solution. A field map is a graphic process in which electric field lines and equipotential lines between two conducting elements are sketched, keeping the curvilinear areas between these two lines approximately square. On the completed map each square is equivalent to one unit capacitor, allowing for the dielectric constant of the medium. The capacitance is then found from a series-parallel summation of the unit capacitors.

The last major type of noise is common ground-impedance coupling. When several digital circuits are returned through a common ground, as in Figure 7, coupling can occur due to the finite impedance of the ground path. di_1/dt and di_2/dt are not necessarily equal.

Voltage drops in the ground impedance caused by the switching of switch 2 must be considered for their effect on switch 1. Again a distinction between harmful and harmless noise must be made because in some polarities the ground noise from switch 2 actually aids the transition of switch 1. In the case of gates, ground noise usually delays the switching of the affected gate only slightly, but in clocked flip-flops, where the clock exists for a short period, this kind of noise may affect the reliability of the triggering. This also illustrates the difficulty of analyzing noise performance in advance since all polarities and combinations must be considered. Voltage drops in a ground system may be readily calculated for a single current source and a single ground path. However, when sources are distributed along the ground path, the effects are not additive and no satisfactory approximation for estimating this effect has been found as yet.

In most practical cases, the largest amount of coupling is brought about by the inductance of the ground path, the alternating-current resistance normally being negligible. For example, a printed-circuit conducting path 0.033 inch (0.8 millimeter) wide by 0.0028 inch (0.07 millimeter) thick and 7 inches (180 millimeters) long will have an alternating-current resistance of approximately 0.259 ohm at 40 megahertz. Unless excessively large currents are switched the drop across R_g will be negligible, even allowing for the proximity effect which might raise R_g by 50 percent. L_g, however, is approximately 0.227 microhenry, which is sufficient to cause trouble in many cases. The voltage drop across the ground-plane inductance is also a function of di/dt. This type of noise is usually the most difficult to control. Proper design of the ground plane helps, but again economics

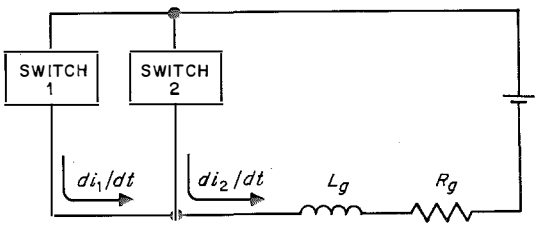

Figure 7—Common ground-impedance coupling.

must be considered. Figure 8 indicates some of the economic considerations of the problem of path sizes. The self-inductance of three different path lengths is shown as a function of path width.

It will be noted that, for a 6-inch (150-millimeter) path, increasing the width from 0.020 to 0.050 inch (0.5 to 1.25 millimeters) reduces the inductance by only 10 percent. Large areas of printed-circuit board will be occupied with an adequate ground return. Splitting the ground path into parallel paths can help, but only where the multiple paths can be physically separated enough to reduce the mutual inductance between them. The same width factor affects the main power distribution system where inductance is also a serious consideration.

The circuit rules generated for the *9100* are based on measurements of actual circuits and wiring configuration. The allowable wiring lengths were set by considering both reflections and possible noise coupling. The noise pickup is the factor weighted more heavily because the noise expected is far less accurately known. Measurements have been made in the *9100* in the range of 0.6 volt of noise (coupled), at times deemed to be harmful, and 0.75 volt of ground noise of the harmful variety. Noise pulses of 1.5 volts were observed but they occurred at times that had no effect on the system as presently programmed. Existence of this amount of noise indicates the need for careful consideration of system noise performance. The *9100* circuits have a noise rejection of 1.6 volts to pulses 25 nanoseconds wide.

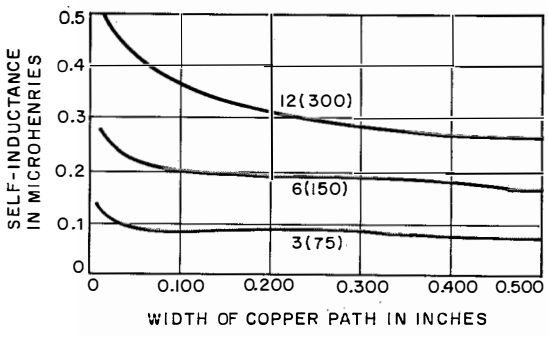

Figure 8—Self-inductance of copper paths 0.0028 inch (0.07 millimeter) thick of indicated width for lengths in inches (millimeters) given on the curves.

It is also of interest that there are two general types of output circuits used in digital microelectronics. They are the single-ended inverter as shown in Figure 9A and the double-ended driver as shown in Figure 9B.

Their behavior under conditions of coupled noise is quite different. In the single-ended case, a positive noise spike coupled in through C_c is clamped to ground if Q1 is on. A negative spike simply adds to logic *0* being propagated (positive *1*'s are assumed here). However, if Q1 is off (putting out a *1*), a positive spike adds to that *1* but a negative spike is potentially dangerous since it subtracts from the desired logic level. The magnitude of voltage actually received is a function of C_c and a parallel combination of R_c and Z_L. Since R_c is often fairly large, considerable coupling can result. In addition, a large R_c often leads to the waveform shown in Figure 10. Even though the succeeding stage has turned on at the break in the rise time (t_b), the circuit recovers its full noise

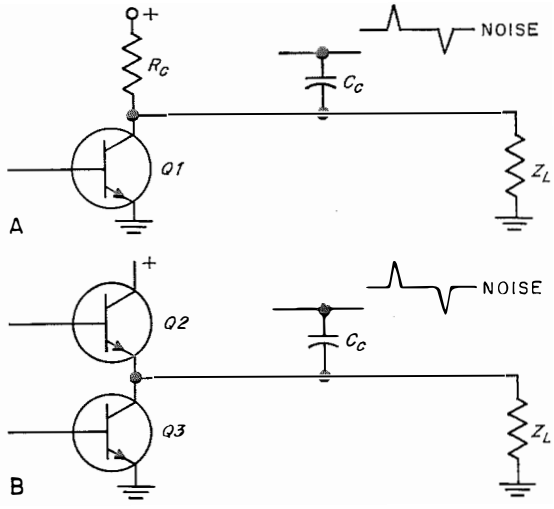

Figure 9—*A* is the single-ended inverter and *B* is the double-ended driver.

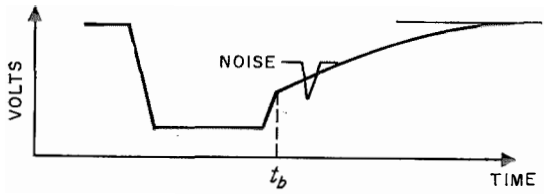

Figure 10—Output waveform from a single-ended driver.

immunity quite slowly and a noise spike arriving as shown is much more likely to cause trouble.

Configuration 9B, however, clamps one end of the line for both polarities of noise unless the noise source places excessive demands for current on the driven transistors. Other considerations must be taken into account when the coupling circuit is too long to be considered lumped, but the principles apply. Configuration 9B has drawbacks though, since it cannot be used in a wired OR configuration, which sometimes leads to a higher number of modules. Also, it cannot be forced to a given logic level, a technique useful in test.

3.2 Figure of Merit for Noise Rejection

Noise threshold is the voltage difference between a normal logic input and the actual threshold of the gate. Thresholds may be either positive or negative depending on whether a *1* or a *0* is being propagated. This threshold is usually expressed in terms of direct-current volts. Because the transient response of a semiconductor switch is limited, the threshold to a narrow pulse is usually higher than the direct-current threshold. This effect becomes apparent at pulse widths of 50 nanoseconds or less, when presently available switches are used.

Since the bulk of system noise consists of sharp spikes, due to the reactance nature of the coupling mechanisms, the noise immunity should be specified in terms of pulse width as well as amplitude. Pulse noise thresholds are measured by determining the pulse amplitude that just brings the driven switch into (or out of) conduction. The measurements thus made are total values. An allowance for the saturation voltage of the previous stage must be subtracted to give a true measure of the spurious noise that can be reactively coupled into the circuit. Luecke [2] and Yao [3] have given a more complete discussion of noise margins in integrated digital circuits although Luecke's discussion is confined to gates. The triggering sensitivity of the flip-flop may be different from that of the gates and must be considered.

To get a true comparison of circuits operating at different voltage and current levels, as well as switching times, we may define a figure of merit that reflects both the noise generating capability and the noise rejection capability of a given circuit. To this end a capacitance noise rejection figure of merit may be defined as (pulse noise threshold)/(dv/dt). A current noise rejection figure of merit may be defined as (pulse noise threshold)/(di/dt). It will be seen that these numbers are positive figures of merit, that is, a large number is more desirable. A circuit with a high noise threshold and a very low slope of voltage change would have a very high figure of merit. It will also be noted that the units of these figures of merit are time based, that is, seconds (or ohm-seconds in the second case). Actually, the units chosen are unimportant; the significant thing is the relative magnitude. As absolute numbers they mean very little, while as comparative numbers they are quite important.

The comparison of two or more lines of digital packages is made more meaningful by this means than a comparison of absolute noise threshold would be, because it relates the noise threshold to the amount of noise to be expected. The physical interconnections would be largely the same whether the packages were *TO5,* flat pack, or dual in-line pack, and the choice between them should have no effect on the noise rejection capabilities of the circuits. In brief, comparison of digital modules for the noise rejection capability must include both the noise

rejection capability and the noise *generation* capability. The foregoing figures of merit tie both capabilities together.

Figures of merit for both types of noise rejection are shown below for currently available digital packages. These values are only representative and are intended to indicate the general range encountered. They can be improved on by selection of circuits for noise immunity but at increased cost. The conventional circuits referred to are diode-transistor-logic circuits assembled from discrete components. They operate on a −3-volt logic level and exhibit a stage delay of approximately 50 nanoseconds.

Noise Rejection Figure of Merit

	Capacitance	Current
Direct-coupled logic	6–8	1–2
Diode-transistor logic	3.5–10	2–5
Emitter-coupled logic (current switching)	3.5–4.5	4–5
Conventional circuits (*ADX* model 2)	5–7.5	3–5.5

In general, microelectronic circuits are about as good as conventional circuits on this basis, but conventional circuits require more noise rejection capability. System noise is a direct function of lead length, and the less-dense packing of conventional circuits requires longer interconnecting wires, both signal and ground. It will be noted that direct-coupled logic is poor in the rejection of current noise (which is the kind encountered in ground planes and is the hardest to control). Emitter-coupled logic, despite the low voltage swing employed, is not as good as some other forms, due to the low thresholds and the relatively larger switched currents. The newer versions are improving in this respect and, since the current always flows in one side or the other, this type of switch is current-balanced and less switched current flows in the power and ground leads.

4. Conclusion

The area of digital system noise has been explored in detail and a means provided for a more meaningful comparison of circuit noise rejection. Further work should be done in improving techniques of estimating noise pickup. Better means of estimating ground-plane noise should also be explored, as well as means for separating the effects of harmful noise from the harmless (which cannot cause a machine malfunction). Finally, further study of economical means of high-density packaging should be made to take advantage of the inherent size of microelectronic modules. The equipment size reduction would be of secondary importance to the reduction of the length of intermodule wiring.

5. References

1. D. Jarvis, "Effects of Interconnections on High-Speed Logic Circuits," *IEEE Transactions on Electronic Computers,* volume EC-12, pages 476–487; October 1963.

2. G. Luecke, "Noise Margins in Digital Integrated Circuits," *Proceedings of the IEEE,* volume 52, number 12, pages 1565–1571; December 1964.

3. F. Yao, "Interconnection and Noise Immunity of Circuitry in Digital Computers," *IEEE Transactions on Electronic Computers,* volume EC-14, pages 875–880; December 1965.

Alex Richardson received a bachelor's degree in electrical engineering from Cornell University in 1951 and a master's degree from Stevens Institute in 1961.

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Microelectronics Applied to an Airborne Photo Data Recorder

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1. Background of Recorder

1.1 Functional Description

The photo data recorder is used primarily in airborne reconnaissance. It provides a means by which aerial photographs of ground terrain can be immediately and easily correlated with the actual time, position, and attitude of the flying vehicle with respect to the earth, and with fixed identification information. Sometimes the same correlation information is required on photographically recorded radar and infrared sensor outputs.

The basic correlation is achieved by means of an information display within the field of view of each camera. The information display usually includes such items as time, latitude, longitude, altitude, speed, true heading, roll angle, pitch angle, date, mission number, and sensor identification number. The flight information is usually obtained in the form of analog signals from inertial or stellar navigation equipment, altitude sensors, or radar measuring equipment, or it may be available in digital form from an onboard computing system or analog-to-digital conversion system. When the information is provided in analog form, it must be converted to digital form by the photo data recorder.

Typically, the information display is generated on a miniature cathode-ray tube in the form of a matrix of dots and recorded in one corner of the photograph as shown in Figure 1. A variety of codes and formats can be used (in-

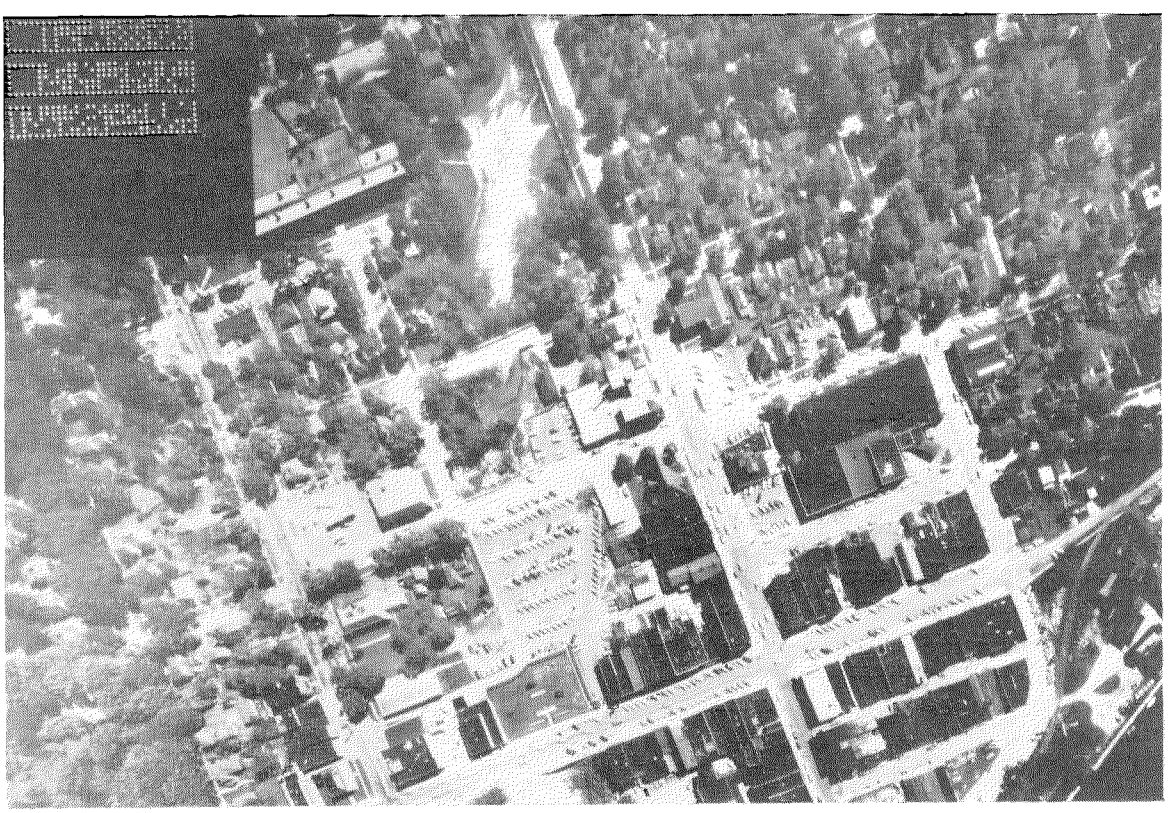

Figure 1—Aerial photo with superimposed code matrix block. To read the code matrix block, rotate the photograph 90 degrees counterclockwise.

cluding alphanumeric characters). In Figure 1, excess-3 binary coded decimal is used and the format is that prescribed by *MIL-STD-782A,* a Department of Defense standard based on recordings produced by several generations of our equipment. Among other things, the data show that Figure 1 was exposed in an aircraft traveling at an altitude of 1060 feet (323 meters) with a true heading of 38.7 degrees. The time was 3 hours, 5 minutes, and 19.1 seconds post meridian on 3 May 1966. The aircraft's position was 86° 17.7′ west longitude and 43° 23.4′ north latitude.

This information is obtained by knowing the location in the format assigned to the various functions and decoding the excess-3 code in these locations. For example, time is contained in the second through eighth horizontal rows in the third column, reading from the top down. Each horizontal row within the column represents one decimal digit. A dot is always present at the right of each digit and is for indexing purposes. The next four dots to the left contain the information in excess-3 code and the extreme left dot in the row is an odd parity bit. Equipment has been built which automatically reads out the complete code block containing 96 decimal digits.

1.2 Physical Description

Over the past 11 years, we have designed and built five different models of photo data recording systems. The first such system was constructed completely with vacuum tubes as active elements. A recent model uses semiconductors throughout, except for the cathode-ray-tube recording head.

The all-transistor version has been in production for over 3 years. It bears the military nomenclature Digital Data System *AN/AYA-1.* A photograph of the system is shown in Figure 2. Its capabilities include outputs for driving 7 cathode-ray-tube recording heads independently. In addition, it provides 3 outputs with different formats for recording on a digital magnetic tape recorder.

Figure 2 shows the 4 major components that make up the all-transistor system. They are the translator, 3-head recording amplifier, 2-head recording amplifier (two shown), and 2-head high-intensity recording amplifier. Also shown are several cathode-ray-tube recording heads.

1.2.1 *Translator*

The largest unit is the translator, which contains all of the digital logic circuits required to accept, arrange, and format the information, then route it to the proper recording amplifier or the tape recorder. The translator also contains a real-time generator with visual and electrical readout and means for inserting fixed information into the data format.

The translator uses diode-transistor logic (*DTL*). Construction follows a plug-in building-block approach in which the building blocks as a rule are functionally peculiar to system requirements rather than the general-purpose logic modules frequently used in digital-computer design. An exception is the use of individual flip-flop boards with set, reset, and complement input terminals. The flip-flops and several other functional circuits are built with

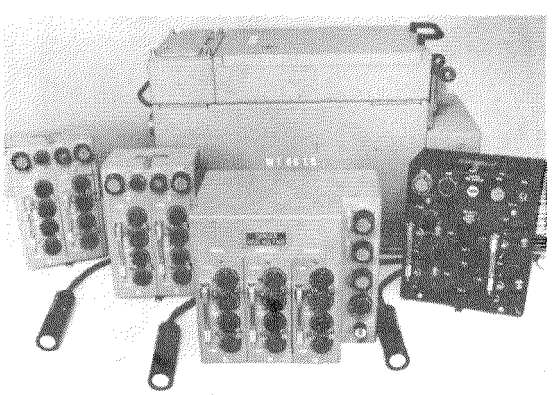

Figure 2—*AN/AYA-1* digital data system. The translator is at the rear with the 3-head recording amplifier centered in front of it. Two 2-head amplifiers are at left and a 2-head high-intensity-recording amplifier is at the right. Several recording heads are shown.

discrete components mounted on 1.75-by-2.25-inch (4.45-by-5.72-centimeter) printed-circuit boards. The flip-flop circuit requires 31 discrete components. Seventy-nine boards of the size of the flip-flop plug into a hinged tray at the top of the translator.

Most of the remaining circuits are contained in twenty 3-by-5-inch (7.6-by-12.7-centimeter) printed-circuit boards and six 5-by-11-inch (12.7-by-27.9-centimeter) boards which plug into the translator from the bottom. Some of these boards have densities of 8 components per square inch. The largest boards are mounted on stiffening trays for vibration isolation.

The real-time generator is an electromechanical device consisting of 7 rotating drums geared together and driven by a synchronous motor. Fixed data are inserted by thumb wheels. All circuits in the translator operate from an 18-volt direct-current power supply that uses 3-phase, 400-hertz aircraft power for primary input.

Cooling is required for operation at an altitude of 75 000 feet (23 000 meters) and an ambient temperature of 100 degrees Celsius. The cooling is provided by an air-to-air heat exchanger supplied from an aircraft air supply, with air internal to the translator forced through the heat-exchanger output side by a high-speed blower.

1.2.2 *Recording Amplifiers*

Located remote from the translator and near the sensor recording stations are the three recording amplifiers. The 3-head recording amplifier contains a power supply of 135 volts for operating all of the amplifiers and ±450 volts for biasing the cathode-ray tubes and providing accelerating voltage.

Each of the three amplifiers contains removable plug-in amplifier modules. There is one module associated with each recording head. Each module contains a horizontal- and vertical-deflection amplifier, a video amplifier, and a potted high-voltage biasing network. Four dials on each module control horizontal and vertical size, intensity, and focus.

The deflection amplifiers are wide-band transistor networks mounted on printed-circuit boards. Each amplifier requires 14 transistors, 8 diodes, 24 resistors, and 8 capacitors. The amplifier puts out approximately 150 volts peak-to-peak and can drive about 20 feet (6 meters) of aircraft shielded cabling with a band pass of 1 hertz to 500 kilohertz. The video amplifier for each cathode-ray tube contains 3 transistors and associated components mounted on two 1-by-1.5-inch (2.5-by-3.8-centimeter) terminal boards. The cathode-ray-tube biasing network is potted with silicon rubber in a 1-by-1.5-by-2-inch (2.5-by-3.8-by-5.1-centimeter) bathtub.

1.2.3 *Technical Characteristics*

The translator has a volume of 2300 cubic inches (37 700 cubic centimeters) and weighs 68 pounds (31 kilograms) including the shock mounts required for vibration isolation. Operation of the translator requires 134 watts of power.

The complete complement of amplifier units with power supply weighs 44 pounds (20 kilograms), occupies 1650 cubic inches (27 000 cubic centimeters), and uses 100 watts of power.

A complete theoretical reliability analysis was done on the system. Under assumed operating environments the failure rates assigned to the nearly 8000 components and associated interconnections resulted in an inherent mean-time-between-failures of 270 hours. When the usual 6.5 "use factor" is applied, this becomes 42 hours. Actual field experience has shown the in-use mean-time-between-failures to be nearly 140 hours.

1.2.4 *System Operation*

Figure 3 is a block diagram of the system. The translator performs all functions required to retrieve data from the various aircraft sources,

process the data, and supply the necessary control signals to the recording head to provide the required display. All logic operations are performed with digital-type circuits. Analog functions use circuits fabricated with miniature discrete components. The translator is configured to accept binary-coded-decimal information from the navigation computer. The

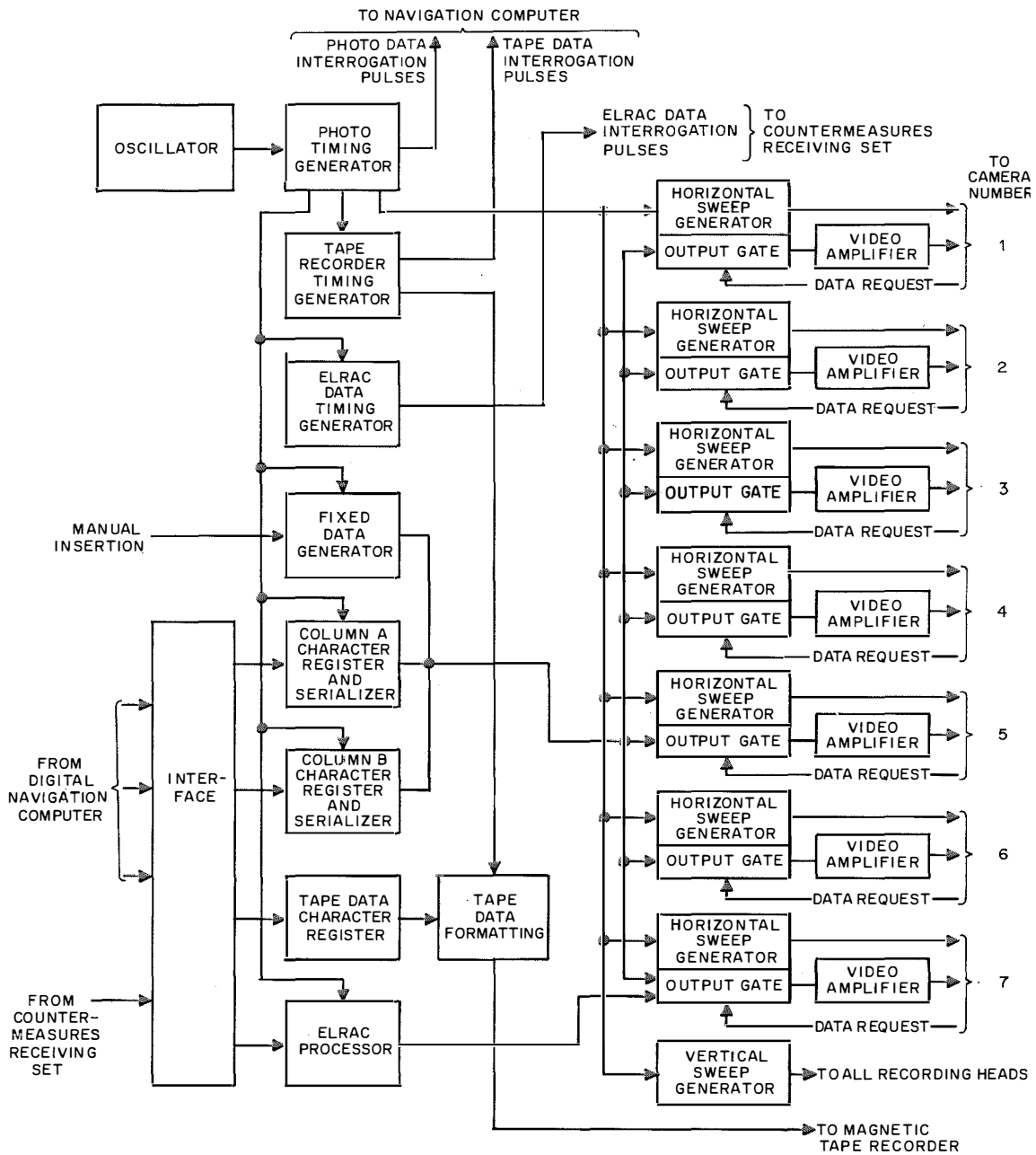

Figure 3—Block diagram of microminiature photo data recorder.

binary-coded-decimal characters are accepted beginning with the least-significant digit of each parameter and ending with the most-significant digit. The navigation computer must supply the following data parameters.

Time	Roll
Latitude	Pitch
Longitude	Mach number
Radar altitude	Ground speed
Barometric altitude	Air speed
Heading	Bomb/Navigation mode
Drift	

The translator supplies parameter selection pulses to the navigation computer on 13 lines. Each line corresponds to one of the parameters listed above. The translator supplies character shift pulses to the navigation computer at a 6.4-kilohertz rate. The levels on these lines are 7.5 volts for a logic *1* and zero volts for a logic *0*. The parameter shift pulse occurs at least 150 microseconds before a character is required. Following the parameter selection pulse, no character shift pulse is sent before readout of the first character of a parameter. Character shift pulses are sent at least 40 microseconds before subsequent character outputs are required. The parameter selection pulses and character shift pulses are 22 microseconds wide and are negative-going.

In response to the parameter selection and character shift pulses, the navigation computer supplies data to the translator (one character at a time) until all characters of the selected parameter have been transferred. The translator accepts data from 3 output registers in the navigation computer. The first output register provides time, latitude, longitude, radar altitude, and bomb/navigation mode. These data are recorded in the first column of the data block. The second output register provides barometric altitude, heading, drift, roll, and pitch data, which will be recorded in the second column of the data block. The third output register provides all of the above data plus true air speed, ground speed, and mach number for recording on magnetic tape.

The system also has the capability of accepting and processing 9 digits of electromagnetic reconnaissance data from a countermeasures receiving set for display and recording in one camera.

When a data request signal is received from the camera in which the countermeasures-receiving-set data are recorded, the translator generates gate and clock signals which are presented to the countermeasures receiving set. The gate pulses have the following characteristics.

On level	= 0 volts
Off level	= 7.5 volts direct current
Pulse width	= 10 milliseconds

The clock pulses have the following characteristics.

On level	= 0 volts
Off level	= 7.5 volts direct current
Pulse width	= 11 microseconds
Pulse interval	= 156 microseconds

On receipt of the gate and clock pulses, the countermeasures receiving set supplies data to the data recording system in the form of a 4-bit binary-coded-decimal character for the digits *0* through *9*. The nine digits of data are supplied in succession by the countermeasures receiving set in response to nine clock pulses from the translator.

The photo data recorder also has the capability of supplying data to a magnetic tape recorder. Data outputs in the form of three unique formats are available on request from the tape recorder and include the information in the data block recorded on the film, plus ground speed, air speed, and mach number.

Provisions are included in the translator for the manual insertion of various fixed data parameters into the tape and photographic data formats. The information is inserted by means of small 10-position rotary switches accessible from the front panel of the translator.

1.3 Design Objectives

In late 1963 it was decided to microminiaturize the system. It will be recalled that 1963 saw the monolithic integrated circuit become worthy of serious consideration for system design. In that year several companies were offering integrated circuits in the standard *TO5* transistor can while two companies had developed the capability of packaging in the now universally used flat pack.

Originally, the degree of miniaturization achievable was rather nebulous. An experimentation phase was undertaken that included fabrication and testing of the standard system flip-flop using thin-film techniques, while at the same time building up some of the other functional circuits using monolithic integrated circuits. This led very shortly to an understanding of the powerful possibilities of the integrated-circuit approach to the microminiaturization of the system.

From this initial work emerged definite goals which were seen to be difficult, though obtainable. The first and major goal was to eliminate the external recording amplifier units so that the complete system (excluding the sensor-mounted cathode-ray tubes) could be contained in a single package. Precisely how this could be done was not clearly seen, but it was considered essential in the equipment improvement program because of maintenance and repair costs associated with any multiunit system.

A second but equally important goal was to reduce the size and weight of the system by an order of magnitude. This meant achieving a weight of from 10 to 15 pounds (4.5 to 6.8 kilograms) and a volume between 400 and 500 cubic inches (6500 and 8200 cubic centimeters).

It was felt that if these goals could be achieved with good engineering practice while keeping the system performance compatible with operation in high-performance military aircraft, an order-of-magnitude increase in reliability would automatically accrue. Although it was hoped, of course, that cost could be reduced along with the other improvements, it was impossible to set a specific target because of the high degree of dependence on future integrated-circuit component cost, which was unknown at that time.

The goals were viewed as reasonably achievable and it was realized that, in addition to the distinct competitive advantage obtainable, new markets could be opened if such a system were actually built. Work was therefore started in earnest.

2. Microminiature System Design

2.1 Elimination of External Amplifiers and Power Supplies

To reduce the system to a single electronics package in addition to cathode-ray-tube recording heads, two general approaches were possible. One was to include the amplifier units in the translator and the other was to include them within the recording-head envelope. It immediately appeared more advantageous to move in the direction of the recording heads, since moving the amplifier closer to the cathode-ray tube reduces the amount of power required to maintain the amplifier bandwidth. Furthermore, enclosing the amplifiers and power supplies within the recording-head envelope offered the possibility of eliminating high voltages from aircraft wiring and reducing the number of interconnecting wires. First consideration was given to this approach.

To accomplish the packaging inside the recording-head envelope without changing its outline dimensions first required that a cathode-ray tube with reduced length be obtained. A tube meeting all the electrical requirements within the size limitations was available from two sources. Use of this tube opened up a cylindrical volume approximately 1.15 inches (2.9 centimeters) in diameter by 1.5 inches (3.8 centimeters) in length in which to package the deflection amplifier, power supply, and bias network.

At first, a theoretical investigation was carried out to determine whether the circuits could be

built up using thin-film resistors and capacitors on a flexible substrate, with miniature transistors and diodes soldered in place on the substrate, and the circuits then rolled up into a cylindrical shape to fit the cylindrical volume available. This approach was abandoned after it was found that depositing thin-film circuits on flexible material was impractical at that time. It was thus determined that the circuits in the recording head would have to be made up of commercially available miniature components wired together and potted in place.

2.1.1 *Miniature Wide-Band Transformers*

It was apparent that a mere repackaging of the deflection amplifiers with miniature components would still require more space than was available. It was therefore decided to try the novel approach of transformer coupling the sweep signals to the electrostatic deflection plates. The success of this approach depended on our ability to wind a transformer with acceptable bandwidth, voltage gain, breakdown voltage, and size. The close proximity of the transformer to the deflection plates was a great asset, of course, because little power would have to be transferred.

The approach was found to be entirely feasible with available materials, although no transformer with such tight characteristics was commercially available. After several attempts a transformer was wound having a voltage gain of 8 with a bandwidth of 1 hertz to 500 kilohertz in 0.75 cubic inch (12.3 cubic centimeters). The small size and wide bandwidth could be achieved because of the extremely high flux densities which the high-permeability core material can carry without saturating. The flux density values achieved are about 75 000 gauss.

Use of the transformers for deflection coupling left approximately 1.25 cubic inches (20.5 cubic centimeters) available to package the high-voltage power supply and biasing circuits. For these purposes a high-efficiency direct-current-to-direct-current converter was designed. The resulting network puts out +900, +450, and −100 volts direct current from an 18-volt direct-current input. This circuit also required a special miniature transformer.

The toroidal transformer is 1.1 inches (2.8 centimeters) in diameter by 0.6 inch (1.5 centimeters) thick and has a secondary-to-primary turns ratio of 56 : 1 with a feedback-to-primary ratio of 0.4 :1. The complete converter operates at a frequency of 45 kilohertz. In addition to the transformer, the direct-current-to-direct-current converter uses 1 transistor, 4 resistors, 1 choke, 4 diodes, and 4 capacitors.

Figure 4 is an exploded layout of the complete recording head illustrating the relative sizes and locations of the components. In its finally assembled form, the components are wired together point to point and the whole rear section is potted in silicone rubber. The design is such that the intensity control can be attached at the rear of the recording head or located at the translator. A completed operating unit is shown with the microminiature translator in Figure 5.

The goals set forth for this design have been achieved. Other system performance improvements that have been achieved simultaneously follow.

(A) High-voltage wiring in aircraft harnesses is eliminated.

(B) High-level sweep and video amplifiers are eliminated.

(C) Elimination of amplifiers and high-voltage power supplies reduces equipment weight and volume.

(D) System reliability and maintainability are improved.

(E) Position, size, and focus controls are eliminated.

(F) Intensity adjustment can be provided at the recording head or camera by controlling the amplitude of a low-level signal.

(G) Operational adjustment and maintenance are greatly simplified.

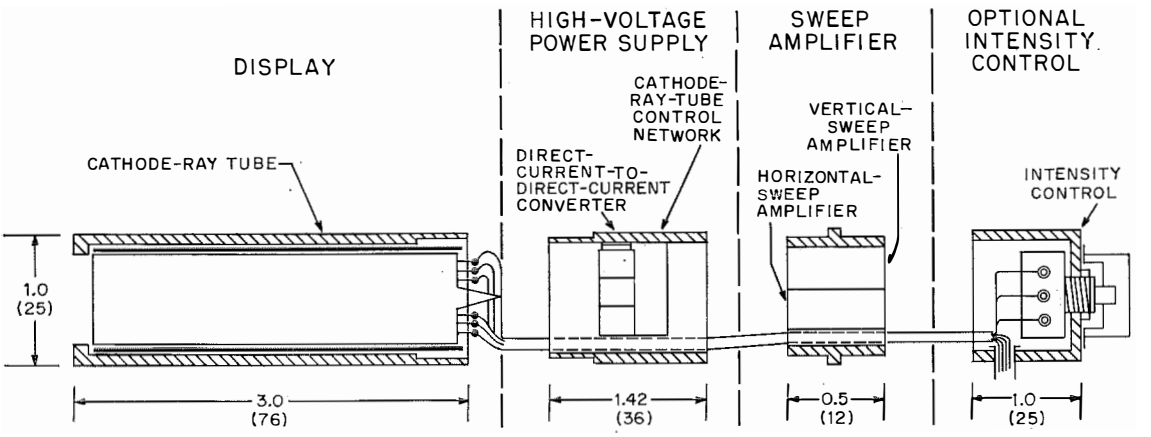

Figure 4--Layout of cathode-ray-tube recording head. All dimensions are in inches (millimeters).

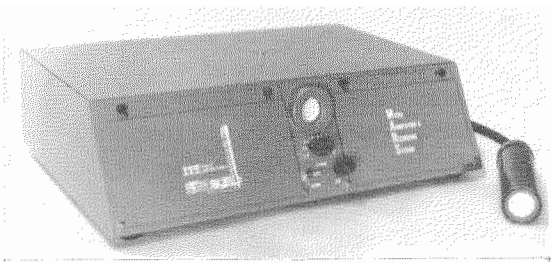

Figure 5—Microminiature translator with cathode-ray-tube recording head.

(H) Complete electrical interchangeability from recording head to recording head can be achieved.

(I) Special applications requiring greater light output, limited range of control, or other variations can be accommodated without affecting the main driving unit. (The recording head can be tailored to a specific application.)

(J) The number of cathode-ray-tube leads required is reduced with the new recording head from 9 to 6.

2.2 Translator Design

By using the low-voltage cathode-ray-tube recording heads described in Section 2.1, the system is reduced to a translator package only. Since the translator is largely a digital unit, application of microelectronic components to the logic sections of the system was accomplished in a straightforward manner. A major part of the design effort involved the selection of particular integrated circuits from those available, the selection of discrete components for analog circuits, and the selection of an efficient packaging configuration.

2.2.1 *Monolithic Integrated Circuits*

The majority of the integrated circuits used in the translator are the diode-transistor-micrologic series supplied by Fairchild Semiconductors. These devices are rated for operation over the full military temperature range of -55 to $+125$ degrees Celsius.

In arriving at this selection, the basic factors involved were a determination of the logic form (diode-transistor logic, resistor-transistor logic, emitter-coupled logic, et cetera) to be used and the manufacturer to supply the devices. Because the original *AN/AYA-1* translator was designed with diode-transistor logic, this type of integrated circuit offered more-convenient direct-replacement capability to make the conversion.

The major emphasis, however, was placed on noise immunity, power dissipation, speed, and

cost of the various devices. In general, each of these characteristics is more nearly fulfilled by a different logic type. It was therefore necessary to make tradeoffs based on system requirements to appropriately characterize the devices required for this application. The tradeoffs were arrived at by considering the following factors which are pertinent to the application.

(A) Noise Immunity—The requirement for a high level of noise immunity was considered the most important factor in evaluating the various logic forms. Experience has shown that the military airborne environment is one of the noisiest in which electronic equipment must operate. A peculiarity of the photo data recorder is the requirement that it be internally interfaced at several points with up to 10 other reconnaissance subsystems located throughout the aircraft. This is responsible for the severe complications resulting from noise generated and transmitted by the various subsystems, from noise pickup along the interconnecting cables, and from the grounding problems prevalent in an arrangement of this type. Operation of radars and transients developed by camera shutters must also be considered.

At the time of this development, the maximum degree of noise immunity was exhibited by the diode-transistor-logic form.

(B) Power Dissipation—A major factor in converting a system from discrete components to integrated circuits is the reduction in input power. A review of the devices available during the design phase revealed that the resistor-transistor-logic and direct-coupled-transistor-logic types had the lowest power dissipation. The emitter-coupled-logic type was characterized by the highest power dissipation. These devices also exhibited a relatively lower degree of noise immunity than the diode-transistor-logic type. The immediate application for which the photo data recorder was designed presents no problem of insufficient source power. Maximum power reduction is, therefore, a general design objective. On this basis and considering the noise-immunity requirement, the best tradeoff favors the diode-transistor-logic form.

(C) Speed—The speed or frequency of operation of digital integrated circuits is normally characterized by the propagation delay through the circuit. During the initial design phase of the system, highest speed was available from the emitter-coupled logic. Since the basic system clock operates at 350 kilohertz, the full capability of the emitter-coupled logic would not be realized. A review of the available devices indicated that all logic forms could meet the system requirements. The major factor involved here is basically one of speed versus power dissipation. Again, the best tradeoff would favor diode-transistor logic for the application.

(D) Cost—In a system using integrated circuits, the circuit components constitute a greater portion of overall system cost than is the case in a conventional system. This was especially true during the early design phases of the microminiature photo data recorder because of the then relatively high cost of integrated circuits over their cost at the present time. Using cost as a criterion in the selection of an appropriate type of logic is difficult at best. Since the device cost is determined largely by the fabrication techniques and the sales volume, both of which are constantly changing, its importance in an evaluation is good at only one specific instant. Assuming a relatively large production run of this system some time after its initial design, the costs of the devices during that period must be known if the greatest economies are to be realized. This knowledge would be predicated on fabrication technology breakthroughs and device popularity, both of which are difficult to forecast.

Considering all these factors, diode-transistor logic clearly offers the best compromise for this application.

2.2.2 Thick-Film Circuits

The sweep generator originally used discrete components including a large number of re-

sistors, and it was determined that film resistors would be desirable to improve packaging efficiency.

Each sweep generator requires a ladder network of 5 resistors whose tolerances and tracking ratios must be kept very close over a wide temperature range. Successful fabrication of these networks would be a true test of manufacturing capability in this area. Generally, the requirements for the ladder network were as follows.

Resistor values in kilohms	(A) 256, 128, 64, 32, 16 (B) 256, 128, 64, 37.1, 37.1
Tolerance in percent	±0.25
Temperature range in degrees Celsius	−55 to +100

It should be noted that two types of resistor network were required. Each network was to be mounted on a single substrate 0.390 by 0.250 inch (0.99 by 0.64 centimeter) in size.

We first attempted to fabricate the units with thin films. These were found to be impractical because of the limited substrate area and relatively high resistor values. It was then decided to fabricate the networks with thick films. This was made possible by recent advances in technology making materials available which exhibited higher resistance values and which were suitable for the screening process. The initial units were fabricated by this process and were found reasonably close to the required values and characteristics. The requirements could be fully met with proper trimming of the networks, and the decision was made to use the thick-film resistors. Figure 6 shows a sample of this network in the lower right-hand corner of the board displayed on the man's palm.

2.2.3 *CHICO Microcomponent Board*

A method of mounting and interconnecting integrated circuits has been developed by ITT Federal Laboratories under the CHICO program (Coordination of Hybrid and Integrated-Circuit Operations), which is a company-funded development of packaging techniques for the use of integrated circuits. The microcomponent board used in the CHICO package was selected for the photo data recorder. The reasons for its selection are outlined below.

The possibility of building an integrated-circuit version of the *AN/AYA-1* digital data system was first considered early in 1963. At that time the various industry approaches to packaging integrated circuits and discrete microcomponents had turned up no really effective configuration. In fact, the most popular approach was to mount the *T05* package on printed-circuit boards that generally consisted of multilayer wiring patterns.

In arriving at a packaging scheme for this program, the alternatives were either to design a better package or to use conventional printed-circuit boards. To design a better package would have required excessive time and cost, plus the cost of implementation (equipment and facilities) for a possible single system.

During the early Fall of 1964, the CHICO packaging configuration was investigated and its advantages over other existing schemes were recognized. It was both simple and efficient. Equipment, personnel, and facilities for its implementation were already being assembled, and sources of supply for needed components were

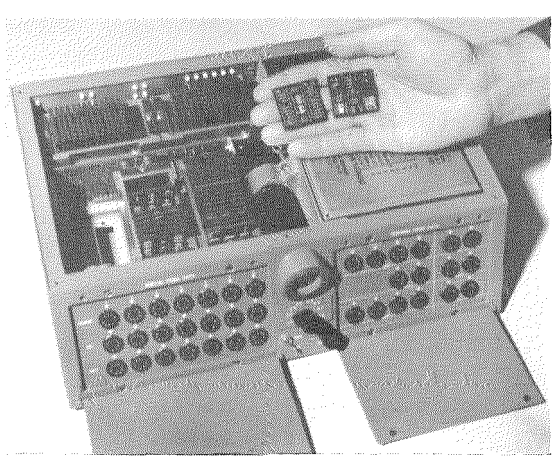

Figure 6—Interior of translator with video amplifier and sweep generator displayed.

being established. In addition, the CHICO approach compared favorably with the cost of a standard printed-circuit-board approach to packaging integrated circuits.

Based on this analysis the decision was made to use the CHICO microcomponent board as the basic integrated-circuit package and also for mounting discrete components required in the system.

Several assemblies were not readily convertible to miniature size by direct use of integrated circuits. These included the video amplifiers (which required higher voltages for system operation) and the sweep generators (which are characterized as analog circuits). Both require line driving capability. Integrated circuits meeting these requirements were not available during system design. A choice was required between use of the existing discrete components or repackaging with miniature components. Since the new low-voltage cathode-ray-tube recording head required extensive modification of the existing sweep generator, it was decided to redesign and repackage this unit with the latest available microcomponents. The existing video amplifier also was found to require extensive changes, dictating a redesign and repackage effort using microcomponents to the greatest extent possible. As a result, only one existing printed-circuit board from the original *AN/AYA-1* was used in the miniaturized system. This board provides highly regulated reference voltages to the sweep generators. Provisions were included in the new system to add this function on a microcomponent board at a later date.

Having decided to repackage the sweep generators and video amplifiers, we needed components which were compatible with the packaging configuration used. The microcomponent boards used in the CHICO package are available in two basic forms, one mounting flat-pack devices and a second mounting a small printed-circuit board which can hold various discrete components including up to six *T05* packages.

It was felt that using discrete components and transistors on the microcomponent boards was not the best packaging approach. It was recognized that the smaller microcomponents becoming available were limited in power-dissipation capability, especially semiconductors and resistors. Of course, the maximum capacitance available in the smaller packages is also limited. These constraints were largely overcome by redesigning the circuits to use the smaller components. In some cases it was necessary to parallel resistors and capacitors to obtain required values and power capabilities. Because of the microcomponent-board spacing within the modules, the maximum component thickness was 0.080 inch (0.2 centimeter). It was found that all needed components were available within this physical limit, including flat-pack transistors.

A decision was made to use the boards mounting flat-pack integrated circuits to package the discrete-component circuits. This approach used the same layout and fabrication techniques for the entire system, thus eliminating the need to lay out additional printed-circuit boards.

2.2.4 *Module Assembly*

When the design effort was started on the miniature photo data recorder, some means of holding and interconnecting the microcomponent boards was required. The basic factors considered in the design of a suitable module included the optimum number of boards, the input/output traffic problems, and the interconnection schemes.

In determining how many microcomponent boards to include in a single module, it is necessary to consider the means by which the boards are interconnected and the possibility of traffic problems. These can, of course, be almost completely eliminated if an unlimited number of layers are used for the interconnecting mother board. The number of boards in the module should also be considered on the basis of a throwaway unit (that is, the level—component,

microcomponent board, or module—at which the cost to isolate and repair a defect equals the cost of the unit). It was felt that it was too early to properly evaluate this throwaway level and therefore this factor did not weigh heavily in the analysis. Examination of the system revealed that modules containing 16 boards would be desirable, as basic subfunctions could be packaged by this number.

To hold the design complexity within practical limits, increase reliability, and reduce costs, multilayer mother boards were ruled out for interconnection within the modules. Even double-layer mother boards caused traffic congestion due to the complexity of interconnections and intraconnections.

At one point an attempt was made to fabricate the entire system in one module containing 64 microcomponent boards. This approach was discarded when it became apparent that interconnection between microcomponent boards would result in excessive traffic on the mother board. The same problem occurred when two 32-board modules were tried. When the system was broken down into four modules of 16 boards each, the interconnection problem proved easier to solve using the double-layer mother board.

Even with four modules, interconnection of module assemblies was difficult because of the large number of input/output points required. The only solution was to bring the input/output leads to the sides of the board. Sufficient paths are available on the board to carry out the necessary interconnections with a minimum of traffic congestion. The input/output leads go to small terminals along the sides of the mother board and from that point are wired directly to two 50-pin connectors mounted directly beneath the mother board. These provide 100 external connections to the module and were sufficient for this application.

The module body was fabricated from aluminum. The sides were milled with grooves which act as guides for the microcomponent boards. The base was machined from solid stock to provide a mounting for the connectors and keying pins. A cover is provided and is held in place by screws which pass through the end plates and secure the module to its mounting surface. Handles are located on the mounting screws to aid in extracting the module. The module is shown in Figure 7.

3. Fabrication Experience

3.1 Microcomponent Boards

The final system design required a total of 60 microcomponent boards. Of this total, 16 boards were largely composed of miniature discrete components while the remainder were used for mounting digital integrated circuits. Twenty-one different artwork patterns were required, and with slight component modifications 23 separate board assembly types were used.

The packaging efficiency of the microcomponent boards in this application is revealed by the fact that the average flat-pack content of the boards performing logic operation is 8.5. The maximum number of 14-pin devices usable on these boards is 9.

The actual fabrication of the microcomponent boards was done at our Microelectronics Laboratory. The fabrication cycle, from submission

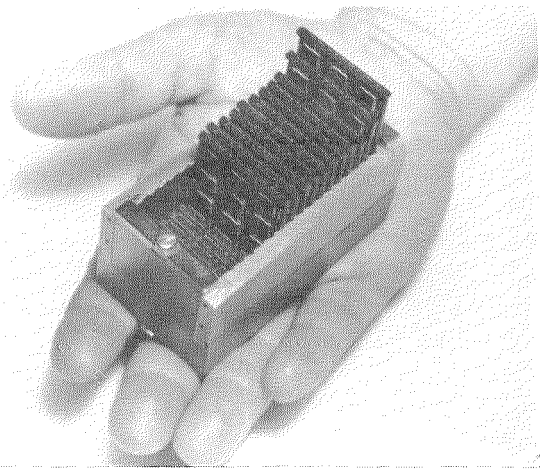

Figure 7—Module assembly.

of the master artwork (assembly drawings and components) to delivery of the finished boards, was handled quickly and effectively. The delivered boards were tested and no defects attributable to the fabrication process have been found. In two cases, defective integrated circuits were assembled on the boards. The reason for these defects has not been determined. It should be noted that the devices are not individually tested before assembly. Based on earlier work along with some breadboard experience with integrated circuits, a high degree of confidence has been established with respect to manufacturer testing of the devices. Our confidence was reinforced by this program, since only two devices out of a total of 500 used in the system were found to be defective after assembly. The defective circuits were isolated within a matter of minutes, and the repairability feature of the microcomponent boards was tested. The defective components were replaced without difficulty and the boards were tested satisfactorily. The time which would have been required to test each circuit before assembly would certainly have been longer than that needed for the isolation and replacement approach used here. On this basis it would appear that appropriate test requirements imposed on manufacturers of integrated-circuit devices would eliminate the need for in-house testing of devices before assembly.

3.2 Modules

No problems were encountered in machining the metal parts of the module.

The mother board was fabricated from $\frac{1}{32}$-inch (0.08-centimeter) copper-clad glass-epoxy printed-circuit-board material. The microcomponent boards are equipped with Cannon Microsocket connectors, each containing 20 pins located on 0.050-inch (0.13-centimeter) centers. Sixteen of the Microsocket connectors are mounted on 0.175-inch (0.445-centimeter) centers on each mother board. Connectors are mounted by passing the 20 dumet leads in the back of each receptacle through plated holes in the mother board and soldering. Terminals are inserted in plated holes along the mother-board edges and soldered. Input/output connection is made by soldering 26-gauge wire jumpers between these terminals and the two 50-pin connectors mounted in the base of the module.

The mother boards were also fabricated in the Microelectronics Laboratory. No difficulties were experienced even with the large number of plated through-holes and conductor widths as small as 0.0075 inch (0.019 centimeter). The modules were wired and assembled by the same department, and system testing revealed no defects or errors.

3.3 Recording Heads

Fabrication experience with the low-voltage cathode-ray-tube recording heads is limited at this time. Feasibility and demonstration units have been assembled on a hand-made basis only.

This experience has proved the feasibility of packaging the necessary components in the desired configuration. It has also shown that additional design effort is required to build an acceptable reproducible package. A number of discrete components are required for the direct-current-to-direct-current converter and control networks. These must be arranged in an orderly manner around the larger transformers. Improved shielding against noise pickup must be provided for signals passing through the various sectors of the recording head. Effective shielding against electromagnetic and electrostatic pickup must also be provided for the cathode-ray tube.

With the experience gained from assembly of the first units, it is anticipated that the use of smaller components and deposited resistors will reduce much of the present congestion. Because of the high voltages and the altitude requirements, the electronics portion of the tube must be potted with a silicone-rubber compound. Provisions must also be made to allow the tube to be replaced when it reaches end-of-life since this should occur before that of the electronics.

4. Accomplishments

The microminiature translator contains four module assemblies with sufficient space for a fifth unit. The modules are mounted on a deck with all interconnection wiring underneath. This portion of the system occupies the left side of the chassis. On the right side is located a power supply that furnishes the four different system voltages. The system input/output connectors, a filament transformer, power control relay, and radio-frequency-interference filter capacitors are also included in the right compartment. The 10-position rotary switches used for manual insertion of various data parameters are recessed in the front panel of the unit. They are protected by the hinged covers which provide access to the switches during preflight operations. A summary of the results follows.

4.1 Volume

The volume of the system was reduced to about 400 cubic inches (6500 cubic centimeters). This compares with 3950 cubic inches (65 000 cubic centimeters) for the discrete-component equivalent. Also, the microminiature unit has sufficient space for another module assembly. Such an additional module would result in a 25-percent increase in the electronic portion of the system. Sufficient power is available from the power supply for this increase.

4.2 Weight

The weight of the microminiature system is 15 pounds (6.8 kilograms). This compares with the original translator weight of 68 pounds (31 kilograms) and a complete system weight including remote amplifiers of 112 pounds (51 kilograms).

4.3 Cost

During the design phase of a program, a considerable amount of the existing circuit design is eliminated while the system logic generally remains the same. In our effort the cost of drafting was significantly reduced. The artwork required much less time for the microcomponent boards than for the usual printed-circuit boards. Experience on this program showed that a maximum of only two days was needed to lay out the most complex wiring patterns of microcomponent boards, with an additional day for taping the master artwork. Mother boards required approximately one week of drafting time for layout and one week for taping of master artwork.

The quantities and types of components are also greatly reduced, thus reducing the number of specification control drawings, planning, and inspection efforts.

Assembly costs for the microcomponent boards and modules have been quite reasonable.

The original *AN/AYA-1* system is presently in production. Recent cost estimates for equivalent quantities of the microminiature version show that it can be built for less. These estimates are based on present prices of the required integrated circuits and, with the continuing reduction in cost of these devices, future system costs will also decrease.

4.4 Performance

The system has been completely checked out and temperature-altitude and vibration tests

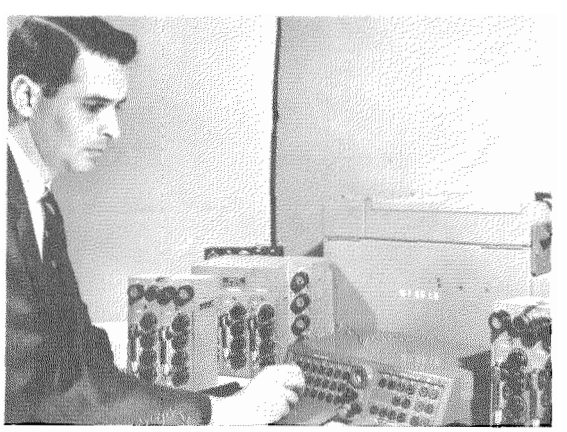

Figure 8—Comparison of microminiature translator (being adjusted) and the *AN/AYA-1*.

have been run. Surprisingly few difficulties (primarily wiring errors in the module interconnection harnesses) have been encountered to this point.

The results of the program to apply microelectronics to an airborne photo data recorder indicate that the design objectives (Section 1.3) were met. Figure 8 contrasts the microelectronic unit (being adjusted) and the original discrete-component version. Weight, volume, and power input have been significantly reduced. The reliability should by all standards increase, although this must yet be demonstrated.

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Microelectronics Microwave Communication Equipment

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1. Introduction

The design of microwave communication equipments and systems for both military and commercial applications continues to reflect all advances in the art. Most recently our emphasis has been on military systems, typical of which is the European Area Communications Plan (*EACP*), a complex of troposcatter and line-of-sight links. This equipment was primarily of vacuum-tube design with solid-state devices limited to low-frequency applications such as video and audio amplifiers. More recently the *AN/TRC-112* solid-state troposcatter equipment was designed and built, representing a significant advance in equipment compactness and reliability.

The need of the military for ever-more compact and reliable systems resulted in our early interest in microelectronics, which was being successfully applied by the industry at that time to digital and low-frequency linear circuits. The general field of microelectronics included monolithic silicon integrated circuits, thin and thick films, pellet circuits, cordwood constructions, and a practically unlimited variety of hybrid techniques.

Film techniques offered a large reduction in equipment size, minimum state-of-the-art performance limitations as applied to microwave communications equipment, and did not involve the huge financial commitments encountered in the design and development of special silicon integrated circuits.

In 1963 a 70-megahertz intermediate-frequency amplifier was developed in which the entire circuit, exclusive of active devices, was designed and built in collaboration with the Physical Sciences Laboratory, using the tantalum thin-film technology. Since that time, pellet components, thick and thin films, standard silicon integrated circuits, and various hybrids have been designed and tested with various degrees of success. These circuits have included all functions, from direct current to 600 megahertz, normally encountered in a microwave terminal.

Late in 1964 a pair of tripod-mounted microwave radio terminals operating in the band from 4.4 to 5 gigahertz were built using primarily thin-film and pellet circuits to demonstrate the size and weight advantages of this type of equipment. This radio set, comprising transmitter, receiver, and order wire, was designated *Pico 1* and was followed in 1965 by *Pico 2,* which uses thick-film circuits in an advanced packaging scheme. The *Pico 2* equipment is the basis for much of this paper, which first lists the advantages and disadvantages of microelectronics in microwave communication, then describes that equipment and touches on the factors involved in designing circuits suitable for microminiaturization including two specific examples. In conclusion, future trends in microelectronic microwave equipment are discussed.

2. Microelectronics in Microwave Communication Equipments

Microelectronics offers the following primary advantages over conventional solid-state circuits.

(A) Greatly reduced size and weight.

(B) Lowered production costs through the use of a greater degree of automatic or semi-automatic fabrication techniques, a smaller and simpler mechanical package, and the elimination of a large number of electrical components.

(C) Potentially greatly improved reliability by the elimination of many of the soldered or welded component connections found in a conventional assembly.

(D) Simplified maintenance. Reducing the cost of modules permits defective ones to be thrown away, which in turn reduces the need for costly repair facilities and skilled personnel.

(E) Improved performance. Reducing the size of circuit elements and the length of interconnections can result in improved circuit performance by reducing parasitic inductance and capacitance and radiation between circuit elements.

The general scaling down of circuit elements possible with microminiature techniques will ultimately permit many microwave functions to be performed by inexpensive miniature microcircuits in lieu of existing cavity structures. Finally, the lower mass of microelectronic equipment is expected to result in improved resistance to mechanical shock and vibration.

The primary disadvantages of microelectronic circuits follow.

(A) Increased development costs due partly to the need for developing special circuit forms

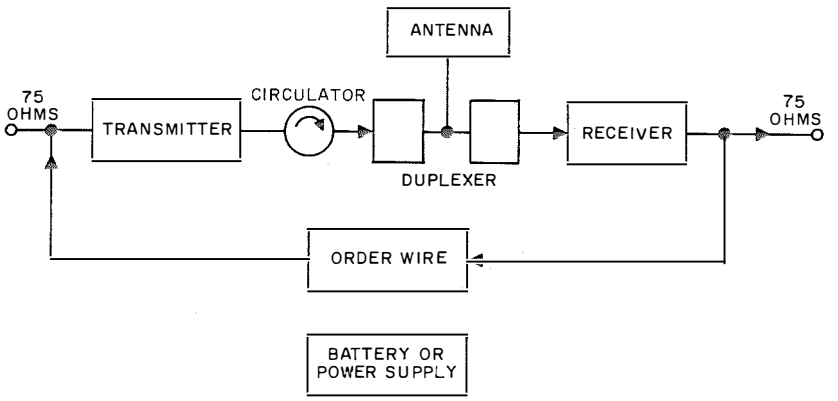

Figure 1—*Pico* terminal.

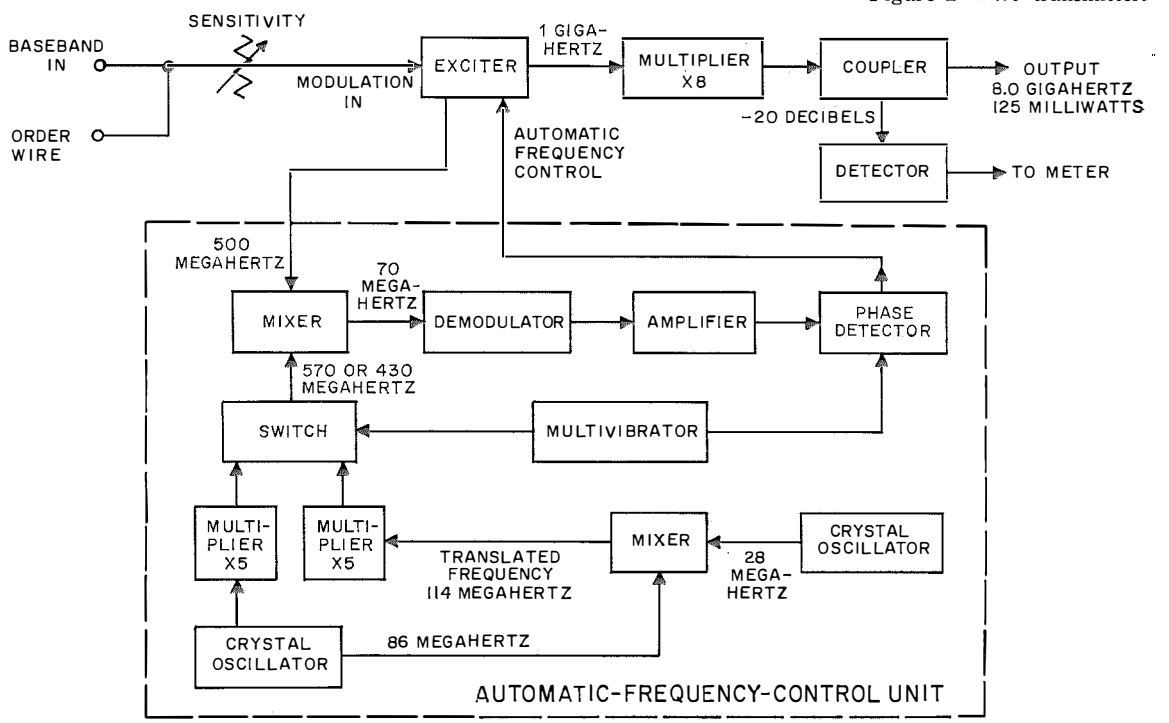

Figure 2—*Pico* transmitter.

suitable for translation in the new medium, and partly to the difficulty of performing circuit development with experimental microcircuits.

(B) Increased cost of making design changes.

(C) Special machinery needed for microcircuit fabrication.

3. Pico 2 Equipment

The *Pico 2* microwave terminal was built to demonstrate the advantages of containing a complete battery-operated line-of-sight radio terminal within a package 13 × 13 × 7 inches (33 × 33 × 18 centimeters) in size, capable of being mounted on a tripod and exchanging television or multichannel traffic with a similar equipment several miles away, with a minimum of setup time by semiskilled personnel.

The terminal includes the transmitter, receiver, antenna, order-wire facility, and power supply, configured as shown in Figure 1. Specifications include the following.

Frequency band (gigahertz)	7.125 to 8.5
Output power (milliwatts)	125
Antenna gain (decibels)	26
Receiver noise figure (decibels)	9
System video bandwidth (megahertz)	6
Channel capacity	300 channels frequency-division multiplex, or television
Operating time	5 hours between battery charges
Size, including batteries	
(inches)	13 × 13 × 7
(centimeters)	33 × 33 × 18
Weight, excluding batteries	
(pounds)	17
(kilograms)	7.7
Order wire	Built-in voice signaling and pilot tone

The transmitter consists of a baseband amplifier, voltage-controlled oscillator (*VCO*), multiplier, and automatic frequency control as shown in Figure 2. The amplified baseband signal modulates a voltage-controlled oscillator which delivers an output of approximately 2.0 watts at 1000 megahertz. This signal is mixed down to 70 megahertz and compared with a crystal-controlled reference. A control voltage proportional to the frequency error and fed back to the voltage-controlled oscillator results in stable transmitter operation. The transmitter design is described in Section 4.2.

The single-conversion superheterodyne receiver configuration is shown in Figure 3. The receiver includes a balanced mixer and local oscillator producing a 70-megahertz output with gain provided by a wide-band intermediate-frequency preamplifier and a main intermediate-frequency amplifier having automatic gain control.

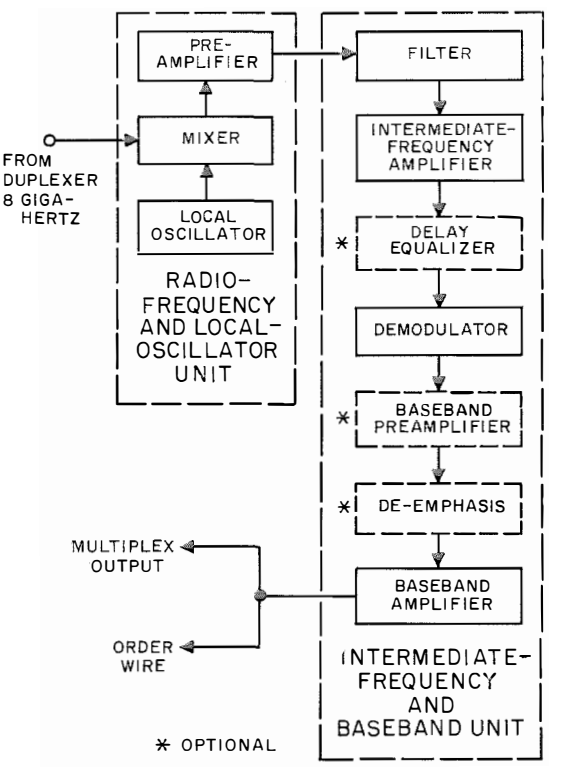

Figure 3—*Pico* receiver.

Plug-in filters provide bandwidths compatible with traffic requirements of the particular application.

Provision for plug-in equalization and de-emphasis modules are included for applications requiring these networks.

Order-wire facilities are provided by a bridging-type circuit which includes talking, signaling, and pilot tone facilities as shown in Figure 4.

The handset transmitter output is amplified and bridged across the radio transmitter input terminals. Also bridged is a 10-kilohertz pilot tone oscillator which is momentarily interrupted for signaling purposes. At the receiver side is an arrangement of low-pass filters to reject the pilot and video traffic and an amplifier which sets the correct handset levels. The pilot tone receiver serves as a pilot alarm and also as a signaling receiver. It operates a bell and a red light in the event of failure of pilot tone or signaling. This system is part of a more complex order-wire design employing conventional in-band signaling circuits and having the following significant features.

(A) Bridging-type circuits to eliminate bulky separation filters, except in baseband repeater applications.

(B) Active filters in place of bulky conventional filters.

(C) Unbalanced circuits to eliminate the transformers formerly required in amplifiers and signaling circuits.

The overall equipment is shown in Figure 5 (rear view showing plug-in assemblies). From left to right, the first panel is a meter and connector panel which swings down to expose the battery pack consisting of nickel-cadmium rechargeable *D* cells arranged in two banks to produce 22 volts and 46 volts, respectively. These batteries discharge through two regulators to produce +15 volts and −37 volts direct current. The space taken by the batteries is also sufficient to accommodate line-voltage power supplies or direct-current-to-direct-current inverter power supplies. The adjacent panel is the receiver radio-frequency and local-oscillator subassembly (Figure 3) comprising the mixer and intermediate-frequency preamplifier and the local oscillator. The next panel is the receiver intermediate-frequency and baseband subassembly, which remains unchanged from one frequency band to another since all the frequency-determining elements of the receiver are contained on the radio-frequency and local-oscillator sub-

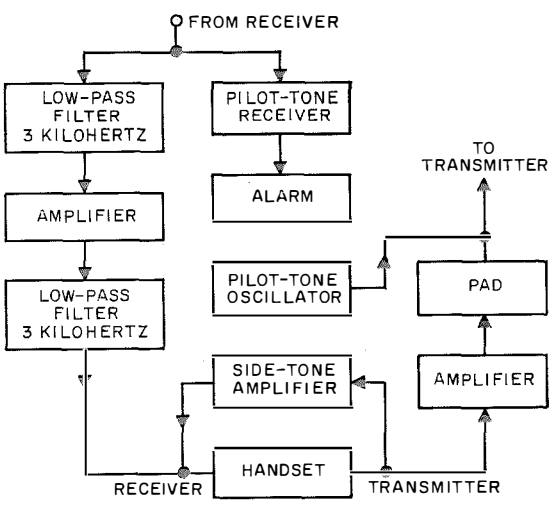

Figure 4—*Pico* order wire.

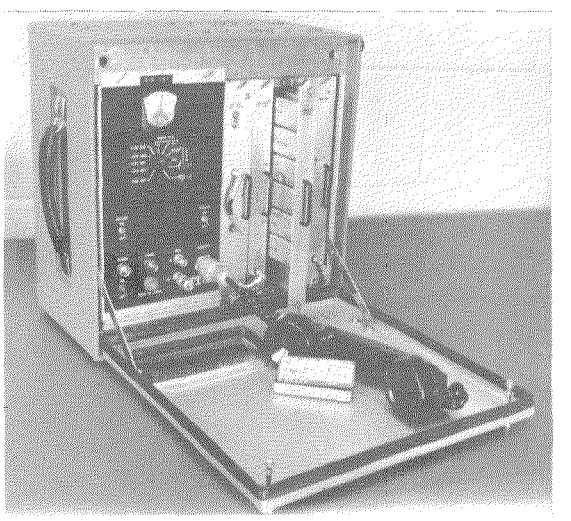

Figure 5—*Pico* terminal.

assembly. The next panel is the order-wire subassembly, followed by the automatic-frequency-control and transmitter subassembly.

The order-wire unit is shown in Figure 6. It comprises a front panel mounted to a wraparound frame supporting a printed-circuit board into which the modules are plugged. Connections to the subassembly are made through one or more connectors mounted at the rear of the module. Each board is capable of mounting up to 7 semistandard modules each approximately $3\frac{1}{2} \times 1\frac{1}{4} \times \frac{5}{8}$ inches ($8.9 \times 3.2 \times 1.6$ centimeters). All subassemblies are approximately 10 inches (25 centimeters) high by $3\frac{1}{2}$ inches (9 centimeters) deep, and only the front-panel width dimension of approximately 1 inch (2.5 centimeters) is changed to suit the different space requirements of certain modules.

The modules themselves consist of a metal header containing up to 26 individually inserted connector pins on standard centers. Riser wires from these connectors pass through holes in the substrate and are soldered to surrounding land areas to make connection to the circuits. A typical module is shown in Figure 7 and a more-complex double-deck module is shown in Figure 8. A can is mounted on the header for shielding purposes and the module filled with a Dow Corning silicone resin for environmental protection. One of the significant electrical features of the *Pico* equipment is the absence of coaxial signal cables between modules. This is made possible by the small module size, which permits short unshielded printed-circuit connections to be used between modules. These connections have a low profile and are very much shorter than $\frac{1}{4}$ wavelength at the critical intermediate frequency of 70 megahertz, hence the radiation or coupling properties and circuit mismatch effects are all minimized. A dishpan is included to shield the exposed circuits from adjacent subassemblies. The complete subassemblies are plugged into a card guide nest contained within the wraparound. The basic nest arrangement is directly applicable to any configuration, tactical or fixed-plant, and would occupy no more than $10\frac{1}{2}$ inches (0.3 meter) of rack height.

The front face of the terminal case is a phased-array printed-circuit antenna with a gain of approximately 26 decibels at 8 gigahertz. This is cable-connected to a waveguide filter-type duplexer which feeds the receiver and transmitter. The receive filter has a bandwidth of 25 megahertz at 1 decibel down, with a rejection to the transmit signal of 60 decibels minimum and an insertion loss of 1 decibel. This filter precedes a miniature balanced strip-line mixer associated with a low-noise 70-megahertz preamplifier capable of being set up with gain of 25 or 40 decibels, compatible with wide-band (high-level) or narrow-band (low-level) system requirements. The preamplifier employs 2 or 3 transistors in a resistor-capacitor-coupled video-amplifier-type configuration with emitter-bypass-capacitor tuning, resulting in a broad band-pass characteristic.

The local oscillator is presently a low-power lumped-circuit oscillator multiplier which will not be described since it is due for replacement. The new unit employs a thick-film crystal oscillator and multiplier with an output at 600

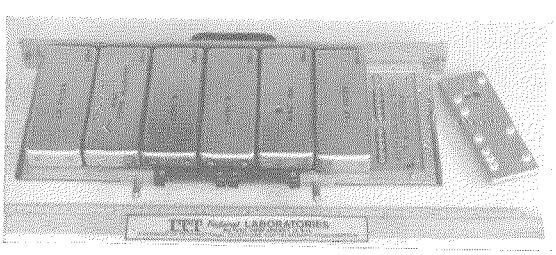

Figure 6—Order-wire subassembly.

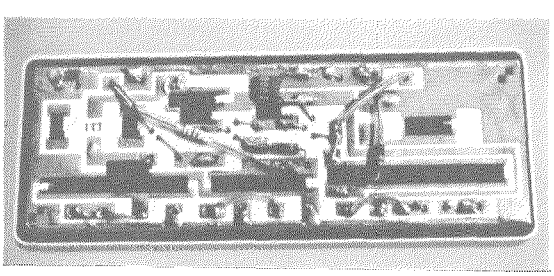

Figure 7—Typical module.

megahertz, which is then further multiplied to 8 gigahertz by a cavity multiplier.

The intermediate-frequency filter is a lumped-circuit two-pole Butterworth filter with a bandwidth of 6 megahertz, employed for general-purpose light-traffic service. This filter is followed by an intermediate-frequency amplifier with a nominal gain of 60 decibels, a bandwidth of 25 megahertz (1 decibel down), and an automatic-gain-control dynamic range of approximately 50 decibels. There are 6 signal transistors employed, and a diode and 3 additional transistors are used in the automatic-gain-control detector and direct-current gain-control circuits. Automatic-gain-control bias is applied to two of the signal transistors to hold the output level constant to within approximately 1 decibel over a 50-decibel input signal range. Circuits are thick-film on two substrates within one $3\frac{1}{8} \times 1\frac{1}{4} \times \frac{3}{4}$-inch ($8 \times 3 \times 2$-centimeter) package as shown in Figure 8. The demodulator is described in detail in Section 4.1. Video gain is supplied by one low-distortion baseband amplifier having a maximum gain of 25 decibels and a bandwidth in excess of 10 megahertz. This unit, shown in Figure 9, is typical of the video and order-wire circuits and employs 3 transistors in an overall feedback circuit that uses thick-film resistors, the number of large add-on capacitors being minimized by direct-current interstage coupling.

4. Circuit Design for Microminiaturization

To most effectively realize the benefits of microminiaturization, circuits must be specially designed to fit within the constraints imposed by the particular microcircuit technology or technologies selected. The thick-film technology was selected for the following reasons.

(A) Low production costs.

(B) Modest screen and sample circuit fabrication costs during engineering phases.

(C) Reasonably short "layout to sample circuit" time cycle.

(D) Relatively rugged circuit elements capable of withstanding normal handling.

(E) Existence of a reliable and suitable capacitor technology based on the long-established ceramic capacitor business.

All thick-film circuits are formed on an aluminum oxide substrate 1 inch (2.54 centimeters) wide by 3 inches (7.62 centimeters) long by 0.035 inch (0.089 centimeter) thick. The circuit interconnection pattern and capacitor ground planes are formed by screening du Pont *7000* series platinum-gold ink onto the substrate, which is subsequently fired in a furnace. Resistors (black rectangular areas on upper panel in Figure 9) are formed by screening and firing du Pont *8000* series palladium-silver inks in selected areas between conductive end pads laid down in the interconnection pattern. Ink of 3000 ohms per square was generally used, with a very conservative design dissipation of 10 watts per square inch (1.55 watts per

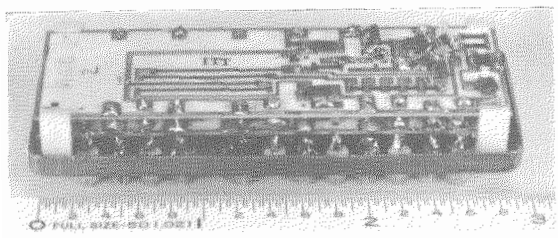

Figure 8—Double-deck module.

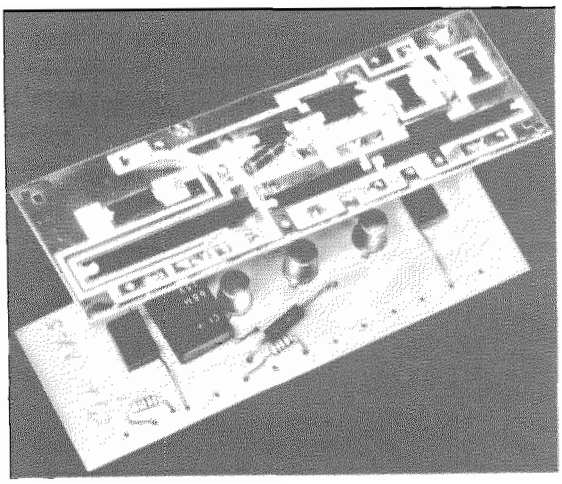

Figure 9—Video-amplifier substrate.

square centimeter). These characteristics result in a 3000-ohm 0.1-watt resistor having both a length and a width of 0.1 inch (2.5 millimeters). The temperature coefficient of these resistors is approximately 14 parts per million per degree Celsius, which compares very favorably with conventional carbon or metal film resistors. A practical range of resistor values of 300 to 1 can be accommodated in a single screening operation by suitably varying the aspect ratios of the resistors. Values outside this range must be accommodated by separate screening operations or by adding conventional resistors.

All resistors are normally designed to be 20 percent below the desired value. The precise values required are then obtained by abrading the sides of the resistor to raise the resistance to the desired tolerance with the help of manual, semiautomatic, or fully automatic equipment.

The capacitors are formed by screening and firing dielectrics of ceramic glass type across the capacitor ground planes originally formed in the interconnection pattern, and then screening and firing capacitor counterelectrodes of platinum-gold over the dielectric areas. The capacitors so formed then provide a capacitance of 2000 to 5000 picofarads per square inch (310 to 775 picofarads per square centimeter), with a breakdown voltage in excess of 100 volts and a Q factor of 1 to 50 at 70 megahertz, the exact characteristics primarily depending on the composition of the dielectric and its thickness. The substrate size of 3 inches by 1 inch (7.6 by 2.5 centimeters) was chosen because of its ability to accommodate the majority of desired circuit functions, including up to 6 low-cost epoxy packaged transistors and a normal complement of add-on components. The substrates are obtained with a special arrangement of holes to accommodate up to 6 transistors in the central area of the substrate and also permit up to 26 connection or mounting wires to be attached near the edges of the substrate. In some cases circuits are formed on both sides of the substrate as shown in Figure 10. This substrate, the intermediate-frequency amplifier, has capacitors on the transistor side and resistors on the reverse side (shown mirrored).

To satisfy the electrical and mechanical constraints imposed by the substrate and film materials, the circuit designers observed the following rules when possible.

(A) Reduce the resistor extreme values to 300 to 1 to avoid multiple screening operations.

(B) Limit capacitor values to 500 picofarads or less.

(C) Minimize the number of inductors (small spiral inductors may be screened on), transformers, trimmer capacitors, adjustable resistors, or other added components.

(D) Generally simplify the design.

The design of two circuits, the 70-megahertz demodulator and the microwave transmitter, will be briefly reviewed to illustrate this practice, which in the case of the demodulator results in a simple, compact, lumped-circuit design.

4.1 70-Megahertz Demodulator

A demodulator design capable of handling up to 600 frequency-division-multiplex voice channels was required comprising limiters, discriminator, and a video output circuit capable of driving a 150-ohm de-emphasis network or video amplifier. Demodulators of this type frequently comprise a series of common-base

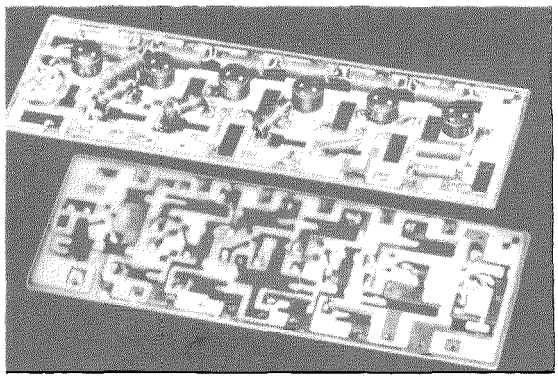

Figure 10—Substrate of intermediate-frequency amplifier.

limiter-amplifier stages with tuned transformer interstage matching networks and a transformer-type discriminator.

To eliminate the matching transformers in the limiter stages, a transistor type *2N918* was selected. This device is capable of providing the requisite stage gain and bandwidth in a common-emitter configuration without matching networks. Three such amplifier stages, employing resistance-capacitance interstage coupling in conjunction with emitter capacitor tuning, provide approximately 40 decibels of limiting with suitable diode limiters. The only essential add-on components are the diodes and transistors.

For similar reasons the discriminator circuit chosen comprised a simple stagger-tuned circuit requiring only 2 transistors, 2 tuning chokes, 2 trimmer capacitors, and 1 adjustable resistor for balancing, as add-on components. A pair of transistors in a direct-current-coupled Darlington circuit buffers the discriminator from the 150-ohm video load external to the demodulator. Additional add-on chokes are used for $B+$ decoupling. A further reduction in the number of add-on components is quite feasible in later models. The microelectronic version of the current design requires two substrates to accommodate the film circuits and add-on components, as shown in Figure 11. The lower deck is the limiter and the upper deck is the discriminator. Riser wires from connector pins inserted in the metal header provide all interconnections between the two substrates as well as making all

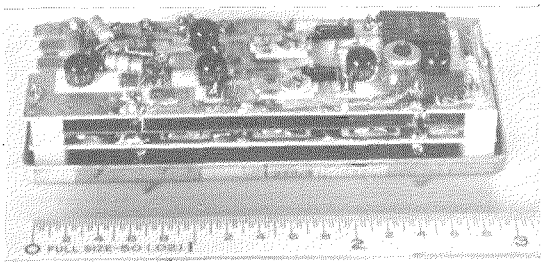

Figure 11—Demodulator.

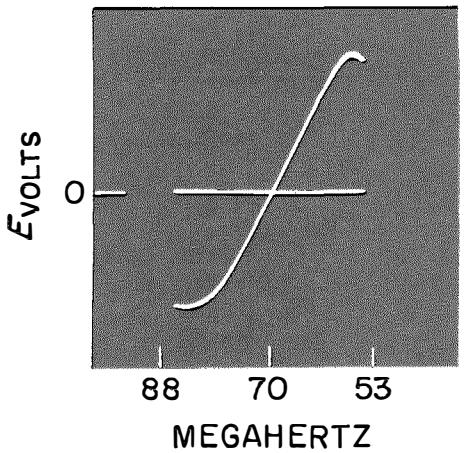

Figure 12—Demodulator swept response. The slope equals 33 millivolts root-mean-square per megahertz.

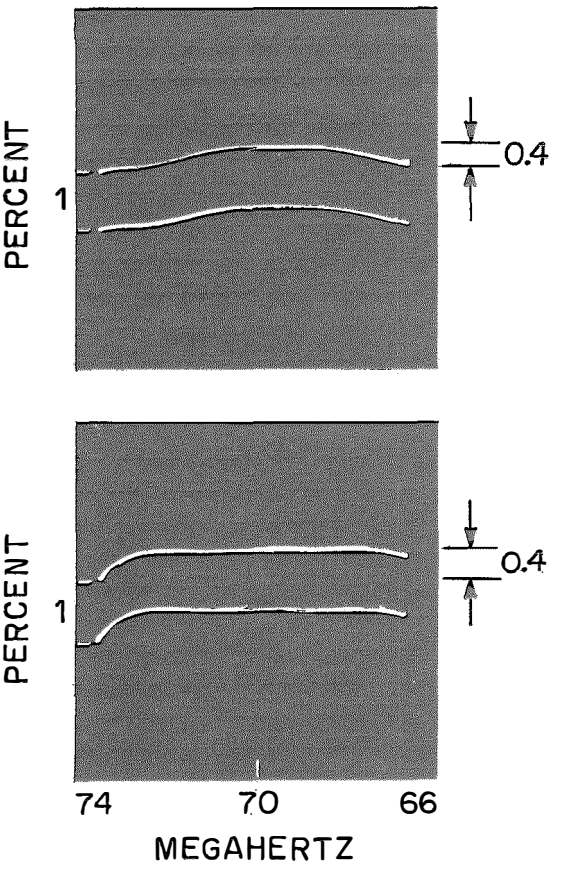

Figure 13—Demodulator incremental linearity. The curves at top are for input of 0.5 volt root-mean-square. The curves at bottom are for input of 0.005 volt root-mean-square.

connections to the printed-circuit subassembly board into which the module is plugged.

Figure 12 shows the swept response of the demodulator, and Figures 13 and 14 show the incremental linearity and group delay at 500-millivolt and 5-millivolt input levels.

4.2 Microwave Transmitter

A compact transmitter was required capable of 125-millivolt output in the band from 7.125 to 8.5 gigahertz with high operating efficiency to minimize power drain. In addition, the design concept was to be capable of supporting up to 600 voice channels or a television signal. Conventional transmitters, employing a crystal oscillator followed by a high-power frequency-multiplier chain with high-level mixing of a 70-megahertz modulated signal, are necessarily inefficient and relatively large. The most efficient configuration for this application was a high-frequency directly modulated power oscillator followed by a varactor multiplier. Automatic frequency control is accomplished by monitoring the output of the 500-megahertz oscillator in a crystal reference automatic-frequency-control circuit, which in turn corrects the oscillator frequency.

A push-pull *2N3375* voltage-controlled oscillator operating at 500 megahertz with doubling in the transistor to 1000 megahertz was designed, with a power output of 2 watts for 12 watts input. This was followed by a separate ×8 varactor multiplier producing 120 milliwatts at 8 gigahertz. For this project no attempt was made to use films in designing the voltage-controlled oscillator, although such application is feasible. However, the power drain and package size were minimized. A photograph of the transmitter subassembly is shown in Figure 15, the voltage-controlled oscillator being identifiable by the finned case.

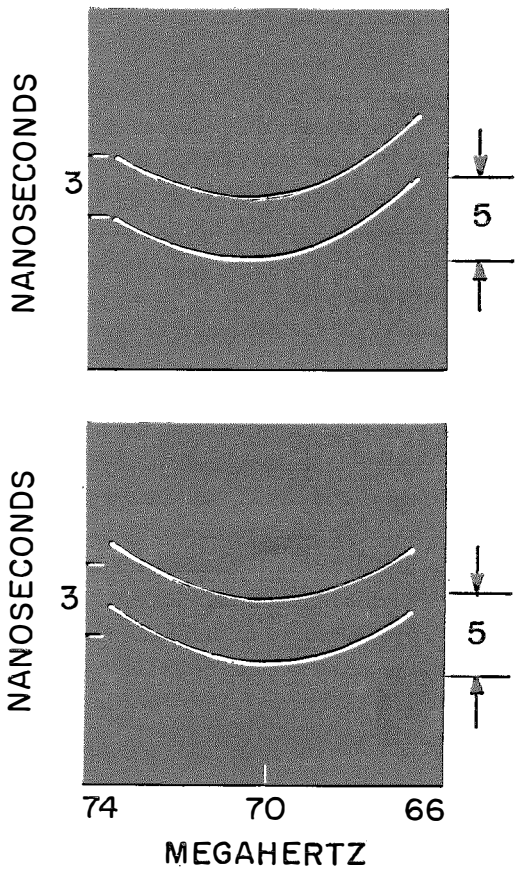

Figure 14—Demodulator group delay. The input voltages are the same as in Figure 13.

5. Future Trends

Before reviewing future trends, it is pertinent to compare a *Pico 2* class of equipment with a

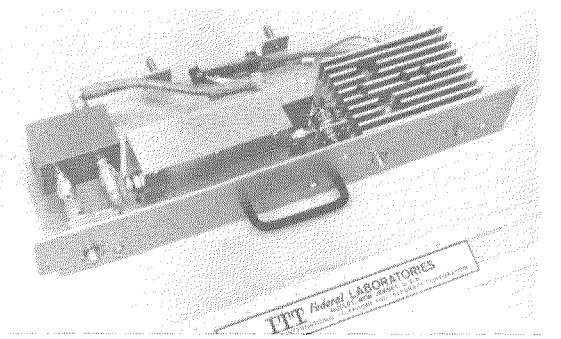

Figure 15—Transmitter subassembly.

roughly equivalent complement of modules from the modern *AN/TRC-112* tactical equipment, which employs solid-state active devices in conjunction with conventional circuits. *Pico 2* represents a 4 or 5 to 1 reduction in volume and an estimated 2 or 3 to 1 reduction in large-quantity production costs.

The separate cabinets of the *AN/TRC-112* radio set, with their separate slides, metering circuits, line filters, wiring harnesses, et cetera, are all combined into one smaller, lighter, and much less costly structure in the *Pico 2* design. This was of course made possible by the initial size reduction of the modules themselves, which suggests that a further reduction in module size could lead to further economies. This is not necessarily the case. The present module size was chosen because it permits low-cost relatively large add-on components such as epoxy packaged transistors to be used. In addition, the reasonably large area available for film circuits resulted in an accurate circuit pattern capable of being reproduced without state-of-the-art screening problems and from artwork generated by draftsmen using conventional drafting materials and procedures.

Further large reduction in equipment size will eventually result from the increasing use of microminiature add-on devices such as flip-chip transistors and diodes, and by the elimination of as many passive add-on components such as chokes, tuning capacitors, and adjustable resistors as possible. This will be accomplished by the design of simpler less-critical circuits requiring fewer adjustments and involving greater feedback, greater bandwidth, et cetera, by using more (and increasingly cheaper) active devices. In much the same way that silicon integrated circuits are presently designed using basically simple circuits and a large number of devices, so will future film circuits tend to be designed, but not to the same extent since add-on active devices will always cost more than integral silicon devices. The advent of successful film transistors could of course change the picture significantly.

In addition to the reduction in size and number of add-on components, the film circuits themselves can and will be designed to take up less area. Size reductions may eventually be limited by considerations such as power dissipation of resistors and the voltage breakdown of capacitors. However, much can be done by starved-circuit design to minimize dissipation problems, and new capacitor dielectrics with improved breakdown characteristics may well be developed. However, present-day film technology is not the primary limiting factor in designs such as this, and further size and cost reductions will be quite feasible with the advent of smaller and less costly add-on components. No problems resulting from the size reduction of critical circuits, such as high-gain intermediate-frequency amplifiers, are anticipated since the critical parameter here is one of proportion rather than absolute size.

As circuits are made smaller and as yields increase, it may be expected that more and more circuits will be combined on a single substrate. This simplification in mechanical structure will in itself bring about a reduction in volume production costs, albeit with a sharp increase in development and capital-equipment costs. Such a trend would ultimately result in small very densely populated substrates requiring automated fabrication, assembly, and test facilities. This trend will not generally be pursued unless high-volume film circuits are required which offer price, performance, or availability advantages over silicon integrated circuits. As silicon integrated circuits become less expensive, they will be increasingly employed in conjunction with film circuits to produce hybrids, in which special circuits are filmed and standard functions are provided by add-on silicon integrated circuits.

Circuits not yet widely converted to film techniques, such as ultra-high-frequency and microwave circuits, will appear increasingly in the near future, and in fact *L*-band circuits involving thin-film resistors and transmission line

structures have already appeared in the literature.*

In general, the suitability of thin films for making precisely dimensioned microminiature lumped circuits with dimensions much less than a quarter wavelength at 1 gigahertz, coupled with the advent of new dielectric (substrate) materials such as low-loss alumina ceramics and new solid-state active devices, will result in a large penetration of the microwave region by lumped-circuit designs.

The *Pico* microwave terminal of the future may therefore be expected to be limited in smallness primarily by fundamental limitations such as antenna aperture (gain) requirements and by the radio-set circuit (primarily transmitter) heat dissipation requirements. It is interesting that the present *Pico 2* equipment, dissipating approximately 35 watts, could be shrunk from 13 × 13 × 7 inches (33 × 33 × 18 centimeters) to approximately 13 × 13 × 1 inches (33 × 33 × 2.5 centimeters) without loss in antenna gain but with a temperature rise of the radio-set case of approximately 23 degrees Celsius above ambient.

Since approximately 12 watts of this power is required by the transmitter and is not significantly reducible by starved-circuit design techniques applicable to the receiver and order wire, this equipment has a certain practical minimum size limited by dissipation and antenna gain requirements. Other such limitations include the minimum size of batteries or power cells, the minimum practical size of operator controls, et cetera. In this context it has been suggested that pygmies be enlisted to operate and maintain future-generation microelectronic radio sets!

* *Digest of Technical Papers*, 1965 International Solid State Circuits Conference, University of Pennsylvania, Philadelphia, Pennsylvania; February 1965.

Charles Greenwald was born on 1 November 1918 in New York City. In 1951 he received a bachelor's degree in electrical engineering from the City College of New York.

In 1944 he joined ITT Federal Laboratories and has worked extensively on defense radio projects. He is now manager of the Circuit and Component Development Group, being responsible for development of microminiature technology applied to microwave communication equipment.

Mr. Greenwald holds membership in the Institute of Electrical and Electronics Engineers.

Basil C. Thompson was born in Maidstone, England, on 7 September 1928. He completed his education in telecommunication engineering at Northern Polytechnic, London, in 1952.

He then joined Kolster-Brandes and in 1957 transferred to the United States to ITT Federal Laboratories in Nutley, New Jersey. Active in the design and development of radio equipment for ground and satellite communication systems, he is now working on broad-band microminiature receivers as a section head in the Transmission Equipment Laboratory.

Mr. Thompson is a member of the Institute of Electrical and Electronics Engineers.

Integrated Circuits Applied to Pulse-Code Modulation

J. V. MARTENS
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1. Introduction

Pulse-code modulation will be used in the near future for military communication in Western Europe. Specifications for pulse-code-modulation equipments are being developed by the *FINABEL* committee, which coordinates the equipment policy of the French, Italian, German, and Benelux Armies.

Our *TU12* multiplex system meets the standard requirements of these specifications, but sufficient flexibility had to be built into the system to cater for alternatives on which a decision is still pending.

Development was started in 1963 in close collaboration with Standard Telecommunication Laboratories and Laboratoire Central de Télécommunications. Manufacturing information for the terminal equipment is available now.

2. Basic Features of *TU12* System

The *TU12* terminal consists of two portable cabinets, one comprising the audio, coding, and decoding circuits for 12 channels, the other comprising the timing generators and the power supply. By adding a second cabinet of the first type, the capacity of the terminal is extended to 24 channels.

The sampling rate is 8 kilohertz, each sample amplitude is quantized into one of 64 levels (6-digit code), and compression is provided to extend the volume range by 20 decibels.

Two alternatives have been foreseen for the synchronizing code: a single-digit code which will be sufficient for point-to-point operation, and a 6-digit code which will be required for operation in an integrated pulse-code-modulation switching and transmission network.

Alternating-current and direct-current signaling facilities are incorporated.

3. Application of Micrologic Circuits

3.1 History

Before development started on the *TU12* system, a preliminary study concluded that the type of logic to be used should be determined first. It was felt that this choice would not only affect the design of the digital circuits but that it might also influence the principles adopted for the entire system design.

Another conclusion drawn from the preliminary study was that the most critical parts of the system are the crosspoints of the analog and digital paths, which are located mainly in the coder and the decoder. Interference from the digital circuits (operating at rather high levels) into the analog path (operating within a broad level range) was expected to be one of the major sources of difficulties. It was therefore decided to separate the instants at which interference could occur from those at which transmission in the analog path becomes effective, and to provide for this purpose two families of timing pulses derived from a double-phase clock.

As a consequence, the system had to be designed around a type of logic compatible with such a clock.

Resistor-transistor logic has finally been adopted, partly because of its simplicity and low cost, but also because a complete family of a resistor-transistor micrologic elements was available. The cost of these latter elements was at that time prohibitive, but they were expected to become fully competitive with conventional circuits in 1966.

Since manufacture of the *TU12* terminals was scheduled to start in 1966 and continue for 3 years, it was decided to design the system in such a way that all its digital circuits could be implemented either by micrologic elements or by conventional circuits of the resistor-transistor-logic type.

For most basic circuits, the final decision between the two alternatives was taken in the early stages of the mechanical design, as a result of a comparative study of the conventional and the integrated-circuit approaches.

3.2 Integrated Versus Conventional Circuits

The major part of the development work was done between the middle of 1963 and the end of 1964. During this period, the information available on the future price evolution of integrated circuits did not provide a firm basis for cost evaluations, especially for the period during which the bulk of components was to be purchased (1966).

Whereas almost general agreement existed on the final price level of integrated circuits, the date at which this level would be reached was subject to discussion. The target date communicated by the supplier (1967) could at that time be considered as overoptimistic. The cost evaluations, which provided guidance in the choice between conventional and integrated circuits, were therefore based on a less favorable evolution, corresponding to approximately one year delay in the target date.

Tentative layouts of the timing generator were made with both conventional and micrologic components to determine the relative costs of mounting. It was found that, using a double-sided printed-circuit board, the cost to mount the conventional circuit for a half-shift register was 20 percent of its purchase cost, while the cost to mount a comparable micrologic element was only 4 percent of its purchase cost.

From all the micrologic elements that could be introduced in the *TU12* terminal, the half-shift register element was the only one for which the evaluation indicated a total cost lower than that of a corresponding conventional circuit.

This element has therefore been introduced systematically (see Figure 1). It is used in all divider stages of the timing generator (two half-shift elements per stage) and it implements the memory functions in the coder and the decoder.

The other elements of the micrologic series have been used when it was necessary to concentrate one complete electrical function on one printed-circuit board to save space, or in circuits where only a small amount of logic could be of the conventional type.

This policy will apparently result in an extra expenditure, especially in early production, but a number of factors that could not readily be introduced in the comparison may finally compensate for the supplementary cost.

These factors are: simple and uniform mechanical layouts, increased reliability, and short connections, with a corresponding reduction of spurious effects.

4. Effect of the New Technology on System Design

Any new system design is based on a rather complex technological background. Relative costs of components, their size and reliability, assembly, and testing facilities are factors that should guide the designer from the early stages of design on paper until the final mechanical layout of the system.

A peculiarity of the *TU12* system is that it has been designed to line up with what is expected to be the technological picture during the manufacturing period (1966–1969).

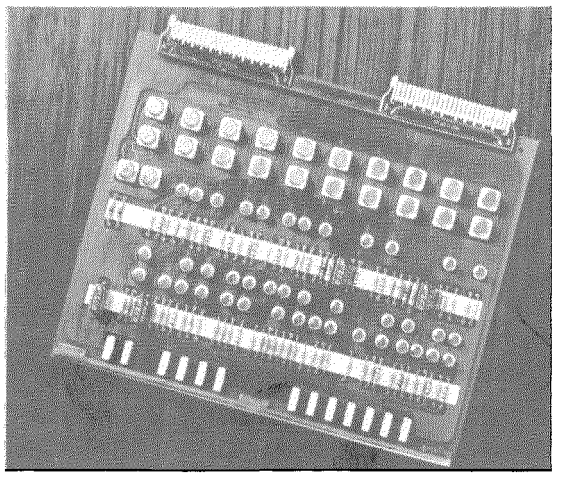

Figure 1—Typical layout illustrating the combined application of micrologic (upper part) and conventional components (lower part). This circuit would require at least two boards if conventional components were used exclusively.

It was foreseen that during this period the cost of conventional semiconductors and integrated circuits would reach its final very-low level and that the reliability of these components would improve. The use of these components was expected to spread widely because of the application of digital solutions to problems that until now were solved by analog methods, plus the penetration of integrated-circuit techniques into analog circuits.

To illustrate these trends two circuits of the *TU12* multiplex will be described.

The first circuit (Section 4.1) is an example of a fully digital approach to both logic and analog problems. One of the purposes of the description is to show that in logic circuit design also, reliability can be increased by a more-complete elimination of analog operations.

The second circuit (Section 4.2) is an example of an analog circuit design made in anticipation of the future introduction of integrated circuits. A characteristic feature of such a design is the extensive use of semiconductors and resistors on the one hand, and the avoidance of reactance components on the other.

4.1 Clock-Pulse Generation

All the timing waves required for sampling, coding, and synchronizing in the transmit circuits of the multiplex equipment are derived by the timing generator from two pulse trains, ϕ_1 and ϕ_2.

The width of the ϕ_1 and ϕ_2 pulses is 110 nanoseconds, and the interval between pulses of the same phase is 870 nanoseconds. Figure 2 represents schematically the generation of pulse trains ϕ_1 and ϕ_2.

Pulses π_1 and π_2 are obtained by differentiating the trapezoidal output wave from a crystal-controlled oscillator of 4.6 megahertz. This is the only part of the system where differentiation is applied.

Timing waves α_M and α_S are derived from π_1 and π_2 by means of two half-shift registers (S1 and S2) operating one as master and the other as slave (Figure 3).

Division by means of two further half-shift registers provides β_M and β_S.

Two flip-flop elements (F1 and F2) are triggered by pulses selected from the π_1 and π_2 trains and provide the ϕ_1 and ϕ_2 pulses. The flip-flop generating ϕ_1 is triggered to 1 by the π_2 pulse for which $\alpha_M = 0$ and $\beta_M = 0$. The

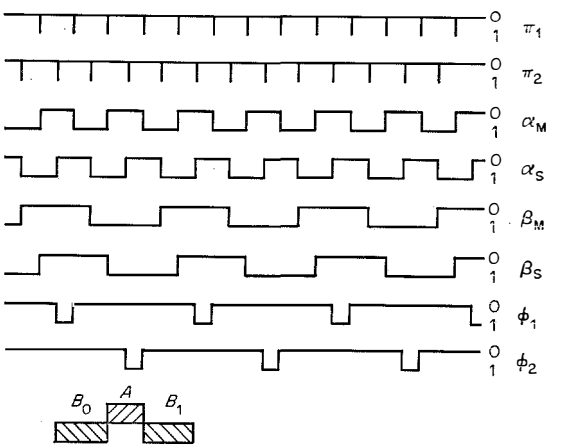

Figure 2—Generation of timing pulses.

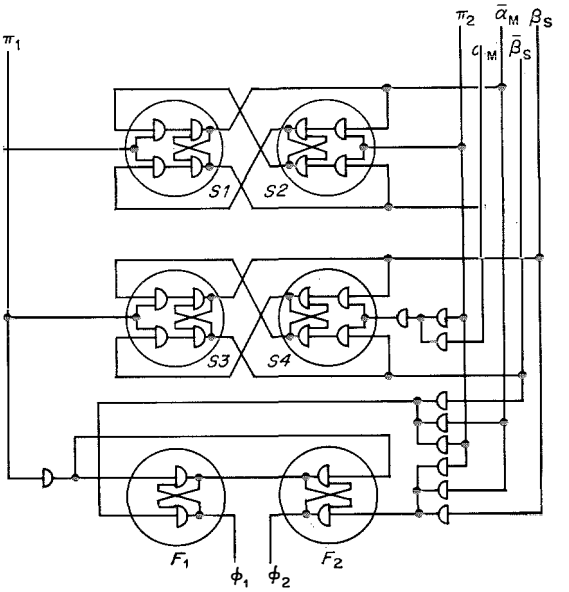

Figure 3—Circuit that generates ϕ_1 and ϕ_2.

flip-flop generating ϕ_2 is triggered to 1 by the π_2 pulse for which $\alpha_M = 0$ and $\beta_M = 1$. Both flip-flops are triggered back to 0 by any π_1 pulse.

The width and the relative position of the clock pulses are thus determined by digital circuits and they remain perfectly stable for temperatures between -30 and $+70$ degrees Celsius.

Similar pulse trains are required for the timing waves of the receive side. However, they should be synchronized with the distant terminal in such a way that one of the pulse trains (ϕ_2 for example) coincides with the transitions of the incoming pulse-code-modulation signal, whereas the other (ϕ_1) determines the instants at which the incoming signal is explored.

In fact, small tolerances of the relative phase of the clock pulses and of the incoming signal are permissible. As long as the transitions occur within area A (Figure 2), the receive clock pulses are derived from π_1 and π_2 in the same way as the transmit clock pulses. A transition occurring either in area B_0 or in area B_1 calls for the intervention of a phasing circuit which either accelerates or decelerates patterns α and β. Acceleration requires admission of an extra π_2 pulse to the half-shift register generating the β patterns and suppression of one of the pulses normally supplied to the elements generating the α patterns. The latter operation alone results in deceleration.

The described procedure differs from that applied in most of the present synchronizing circuits. It consists of extracting the timing information from the pulse-code-modulation signal by means of a narrow crystal filter. The synchronizing circuits include an important analog part in contrast to the described circuit, which could be built entirely by means of integrated digital circuits.

4.2 Compression and Expansion

In the *TU12* system, compression of the high levels is achieved by reducing the gain of the coder input path. This path contains an amplifier that can be switched during coding from high gain to low gain under the control of the first code elements. Figure 4 is the schematic diagram of this amplifier.

It comprises a source of constant current (Q0), plus a switch (Q1, Q2) that directs the available current to the upper (Q3, Q4) or lower

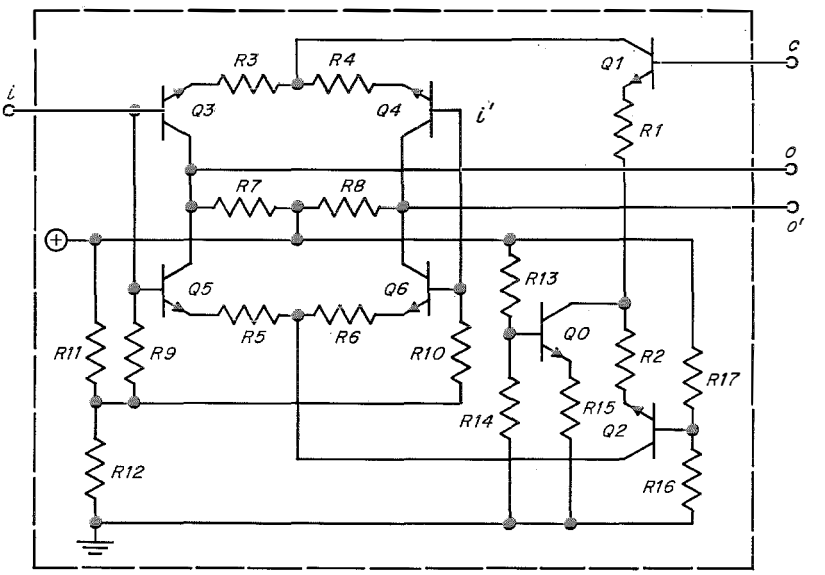

Figure 4—Diagram of switched amplifier.

(Q5, Q6) amplifier path and so determines which of the amplifier paths is active.

The two amplifiers have a common output circuit (o, o') and separate emitter circuits.

When the upper amplifier is active the amplification ratio approximates R7/R3 = R8/R4, and when the lower amplifier is active it approaches R7/R5 = R8/R6.

This circuit contains one of the transfers from analog to digital operation that were mentioned earlier as the critical points of the system.

Owing to the constant-current feature and the common output circuit, decoupling between the control voltages applied to c and the output o, o' is almost perfect.

Furthermore, the output voltage is used for coding, 435 nanoseconds after the gain has been modified, because of the double-phase principle. Any transient that might have leaked into the analog circuit is considerably attenuated during this interval.

The circuit of Q0, Q1, Q2, R1, R2, R13, and R17 has been designed in expectation of its future replacement by a single integrated-circuit element.

Transistors Q3,Q4 and Q5,Q6 are monolithic pairs, but the associated resistors cannot be integrated because of the required precision.

At the receive side, an identical amplifier arrangement provides the complementary expansion characteristic.

The circuit described is typical for the main part of the common transmission paths of a modern pulse-code-modulation multiplex system. In fact, these paths will mainly consist of a tandem connection of similar direct-coupled circuits.

The difficulties that in former systems were due to interaction between control and transmission paths and to the drift of transistor characteristics have been easily solved by the use of monolithic transistor pairs and resistor-transistor circuits.

John Martens was born in Antwerp, Belgium. He received a degree in electromechanical engineering in 1941 and joined Bell Telephone Manufacturing Company one year later. He has worked in the transmission division since that time.

Vatican City Pentaconta Telephone Exchanges—The first 2 of 7 Pentaconta telephone exchanges to serve Vatican City were cut over recently. The main center shown in Figure 1 is in the Vatican itself and replaces the previous rotary exchange. It is equipped with 2000 subscriber lines and 160 city trunks.

The first of the 6 secondary centers was inaugurated in San Giovanni in Laterano and is equipped with 400 subscriber lines. The two exchanges are connected by 44 tie lines and a radio link. Multifrequency signaling is used.

The main center handles its own both-way city traffic and that of the secondary center and later will handle traffic among the secondary centers. City subscribers can dial directly into the Vatican City network using 7 digits and can call the Vatican City operator by dialing 4 digits, the fourth being 2.

City message metering employs an individual meter per subscriber, and toll message metering for outgoing city calls is established by operators using meters with reset to zero individual per city trunk.

Special services obtainable from the main center include time, philatelic information, and Pontifical Ceremony information. They are available to subscribers by dialing 2 digits, the first being 1.

Fabbrica Apparecchiature per Comunicazioni Elettriche Standard
Italy

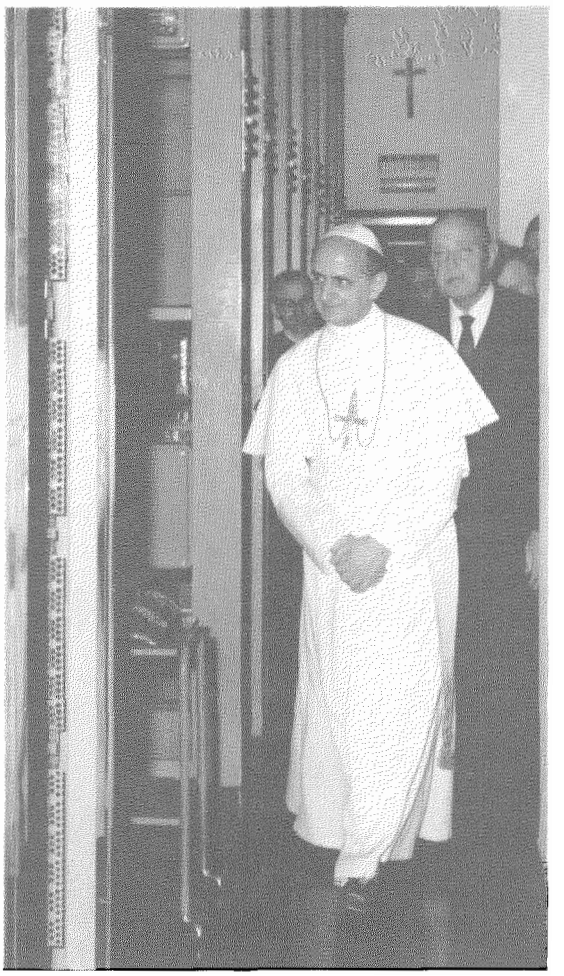

Figure 1—His Holiness Paul VI visiting the new Vatican City telephone exchange.

Lyons National Interurban Center Cut Over—A new automatic interurban exchange, Lyons-Sevigne, was cut over in May 1966 as shown in Figure 2. This Pentaconta crossbar exchange is the first of its type outside of Paris. Its present capacity of 1600 inputs and 1600 outputs will be tripled within the next 3 years.

All switching uses 4-wire circuits. The connections between 4 wires and 2 wires are in the auxiliary lines handling the links with urban exchanges. The new center handles all outgoing traffic from subscribers in Lyons toward the French network, terminal traffic toward subscribers in the Lyons area, and transit traffic as Lyons is a main transit center. An international automatic exchange for outgoing, transit, and incoming traffic will be added next year.

New methods of traffic observation have been introduced. The use of 4-wire operation permits reduction of the overall attenuation between the input and output distributing frames to about 0.05 neper. Internal signaling is over both

transmission circuits through center-tapped inductances, which introduces an attenuation of only a few millinepers.

Compagnie Générale de Constructions Téléphoniques
France

Hydrophones Precisely Positioned for Underwater Tracking Range—Tongue of the Ocean is a valley-like underwater depression about 100 miles (180 kilometers) long and 20 miles (35 kilometers) wide that was selected by the United States Navy as its Atlantic Undersea Test and Evaluation Center. It provides deep water in a relatively quiet sea environment and is close to suitable land masses, the Bahama Islands.

A network of precisely placed hydrophones and some 600 miles (1080 kilometers) of connecting cables permit signals from test devices to be detected and transmitted to data processors on shore. The real-time locations of several targets will be displayed simultaneously.

An underwater communication system will provide for voice transmission between shore facilities and submarines in the test range.

The precision required for hydrophone placement calls for a special cable-laying ship. The *F. V. Hunt,* chartered from Miami Acoustic Services, is a twin-propeller diesel-powered vessel equipped with electric propulsion units on both sides of the stern and bow. These auxiliary units permit precise positioning of the ship despite winds, waves, and currents. A view of the bow deck is given in Figure 3.

ITT Federal Laboratories
United States of America

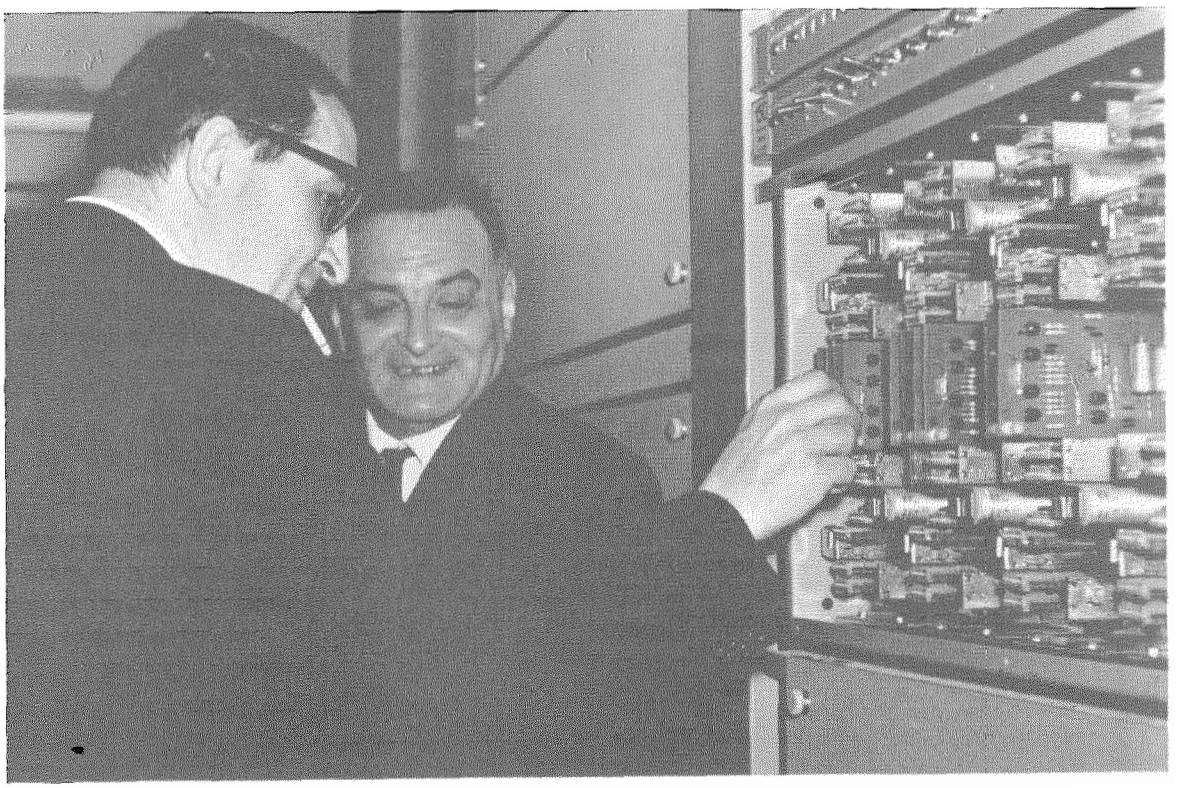

Figure 2—Postmaster General Marette (left), and Area Director Rousselet at the inauguration ceremonies of the Lyons-Sevigne center.

Instrument Landing System Meets Requirements for Category II Operation—The *LK2, LGB,* and *LMB* are the ground equipments for an instrument landing system for aircraft. They meet the full requirements of the International Civil Aviation Organization for Category II operation. This category permits instrument approach with a minimum visual runway range of 400 meters (1300 feet) and a decision to land or abort being made at 30 meters (100 feet) in altitude. A photo of the localizer antenna may be seen in Figure 4.

Standard Elektrik Lorenz
Germany

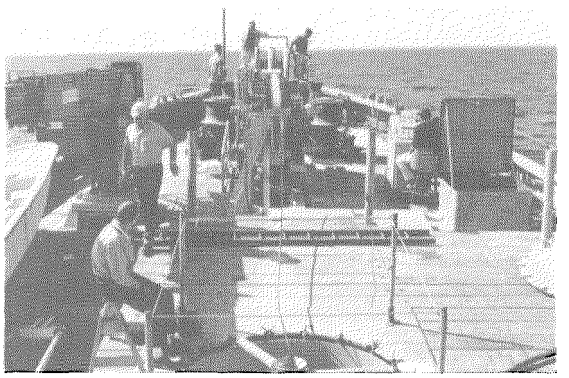

Figure 3—On the *F. V. Hunt* the hydrophone cable stored below deck passes through a cable transport and over the bow sheave for laying. The slack in the cable indicates a momentary "hold" in operations.

Pentelex Private Automatic Telex Exchange—The Pentelex *24* telex exchange is a crossbar system using Pentaconta multiswitches and relays. Plug-in connectors mounted on swing-out frames provide full accessibility from the front of the cabinets. Meeting the international requirements for voice-frequency channels, it provided for half-duplex operation at 50 bauds using the number 2 code. It uses a combined start-stop keyboard. Remotely located teleprinters may be interconnected. Provision can be made for broadcast calling with stations grouped in 10 different combinations and any line can be arranged to have either full or no access to the broadcast service. The keyboard is used for calling.

The capacity of this private automatic exchange is 24 extensions with 6 simultaneous connections. An extension may have a maximum loop resistance of 2500 ohms including the teleprinter and a minimum leakage resistance of 20 kilohms. Operation is satisfactory between 44 and 56 volts. The compact floor-type cabinet includes the power supply and distributing blocks.

Bell Telephone Manufacturing Company
Belgium

Submarine Cable for Space Program—A 760-nautical-mile (1407-kilometer) submarine cable system will connect Cape Kennedy on the

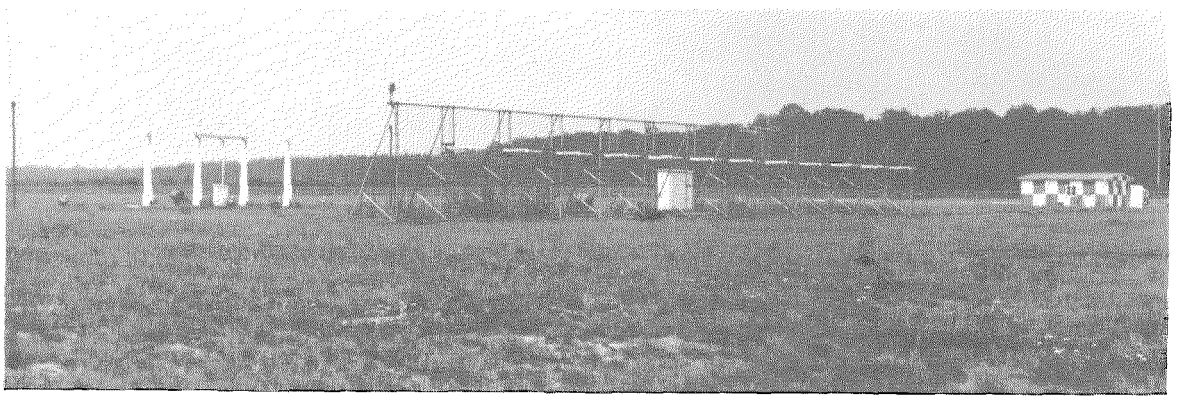

Figure 4—Localizer antenna for aircraft instrument landing system.

Florida coast of the United States with Grand Turk Island. Intermediate stations will be at Grand Bahama Island and San Salvador Island. Between Cape Kennedy and Grand Bahama Island, the cable will carry 270 channels with repeaters every 9.7 nautical miles (17.5 kilometers). The remainder of the system will be equipped for 60 channels with repeaters every 30 nautical miles (55 kilometers). It will be part of the global network for the space exploration program of the United States Air Force and the National Aeronautics and Space Administration.

The cable will be of the latest design using an inner steel-wire strength member enclosed in welded copper tape serving as the inner conductor. This is covered by extruded polyethylene dielectric, which can be seen in Figure 5. An outer copper conductor will then be applied and a final sheath of polyethylene will protect the cable. The submerged repeaters and the terminal multiplexing equipment will be supplied with the cable.

Standard Telephones and Cables
United Kingdom

GH-121 Voice-Frequency Telegraph Equipment—The Swedish Telecommunications Administration has recently ordered modems for about 3000 voice-frequency telegraph channels. As shown in Figure 6, a single-sided bay accommodates 3 self-contained 24-channel modems with a telephone handset and equipment for measuring voltage, current, level, and time distortion.

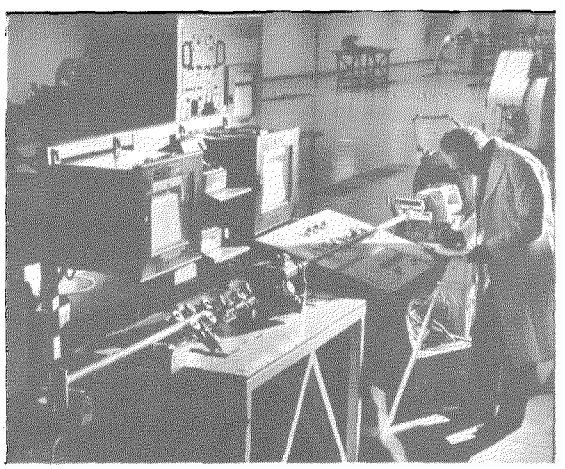

Figure 5—Monitoring the diameter of the dielectric of the submarine cable before applying the outer conductor and sheath.

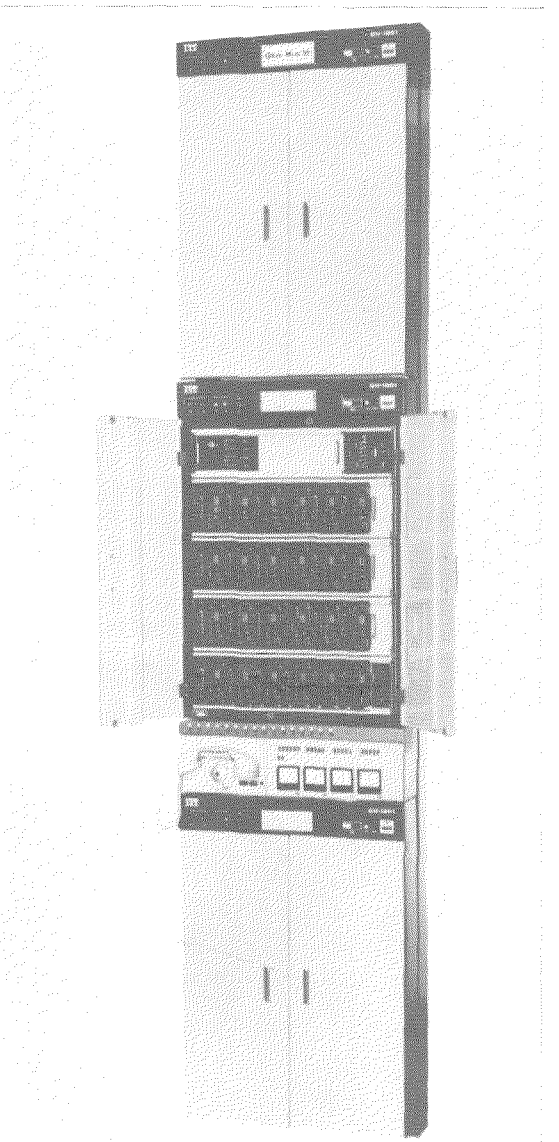

Figure 6—Single bay equipped with 3 voice-frequency 24-channel telegraph modems and monitoring equipment.

Channels may operate at 50, 100, or 200 bauds, even intermixed. Bias correction introduced in each channel receiver compensates for offset of the receive frequency of ±10 hertz.

The *GH-121* is the third generation of a system standardized in 1953 by the Administration, which has used our equipment exclusively for the voice-frequency telegraph equipment in the Swedish telex and telegraph network. This system is also exported to Finland.

Standard Radio & Telefon
Sweden

Pilot Measurement for Carrier Systems—The trolley-mounted equipment shown in Figure 7 includes a precision measurement receiver, signal generator, and power supply operating from the 220-volt alternating-current mains. The receiver measures the pilot signals used for continuously monitoring the transmission lines and repeaters of a multichannel telecommunication system. Level measurements are not affected by existing voice or signal voltages on the system.

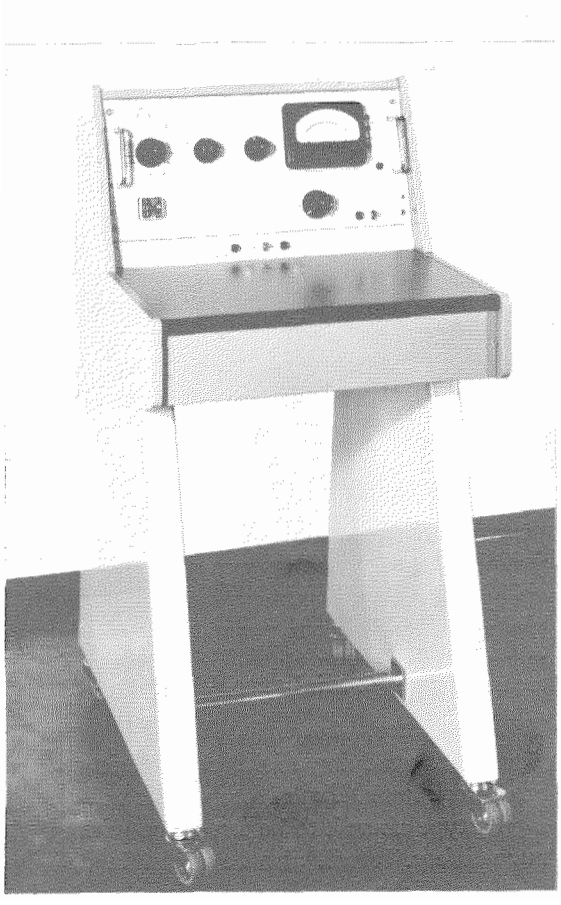

Figure 7—Trolley-mounted pilot-measurement set.

Measurements can be made at the following frequencies in kilohertz, where $\delta = 80$ or 140 hertz: $36 \pm \delta$, 60, $84 + \delta$, $132 + \delta$, $152 + \delta$, $180 + \delta$, $228 + \delta$, 256, $336 - \delta$, $384 - \delta$, 412 $- \delta$, $432 - \delta$, $480 - \delta$, $528 \pm \delta$, and 556.

There are 13 level measurement ranges in steps of 1 neper from 0 nepers referred to 1 milliwatt to −12 nepers referred to 1 milliwatt. For 75 ohms the input is single ended and for 150 ohms it is balanced; in both cases the return loss $\geqq 3$ nepers and zero level is 1 milliwatt. The level-indicating instrument is graduated coarsely from −3 to −1 neper and in 0.02-neper units between −1 and +0.6 neper. It requires 0.9 milliampere for zero-level indication.

The selectivity is such that a signal moved 60 hertz from resonance has a reduction in response $\geqq 4.6$ nepers and $\geqq 7$ nepers for 100 hertz off resonance.

Standard Téléphone et Radio
Switzerland

Madrid Factory Converting to International Standard Equipment Practice—The market requirements for manufacture of transmission multiplex equipment now make it desirable for the Madrid factory to employ the International Standard Equipment Practice. Equipment will be mounted on shallow-type bays 520 millimeters (20 inches) wide.

Personnel are being trained in new assembly techniques and programmed automatic testing devices are in operation. The flow of materials has been planned to avoid unnecessary storage during processing.

Standard Eléctrica
Spain

Laser Beam Transmits Speech in Televised Demonstration—The French television network demonstrated speech transmission over a laser beam on 27 May 1966. The equipment is shown in Figure 8.

An argon laser emitting blue light (4880 angstrom units) was modulated by speech signals from a telephone line. Potassium dihydrogen phosphate was used as the modulator and the modulated laser beam was demodulated by a photomultiplier.

In the demonstration the transmission path was only a few meters long although in clear weather transmission with this equipment has been successful over a few kilometers. No attempt was made to demonstrate the enormous traffic capacity of a laser beam.

Laboratoire Central de Télécommunications
France

Russians See British Equipment—Among the navigation aids displayed at the July exhibition held in Sokolniki Park in Moscow was the *STR-70-P* radio altimeter. It uses monolithic microcircuits and has a mean-time-between-failures of 5000 hours.

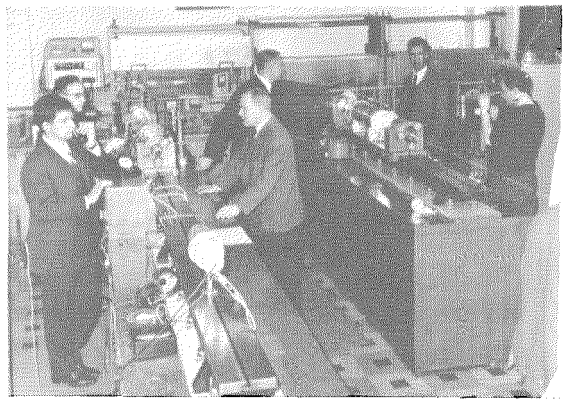

Figure 8—View of the Laser Research Laboratory of Laboratoire Central de Télécommunications just before the television presentation. The laser at the left was used for speech transmission while the more powerful unit to the right projected a laser beam on a wall outside the laboratories.

The Deltaphone telephone handset that won the award of the British Design Centre, a 300-circuit small-coaxial-cable dependent transistor repeater having a bandwidth of 1.3 megahertz, and a multiplexing equipment for handling 2700 telephone channels were also displayed.

The *8300 ADX* and *6300 ADX* computer-based message and data switching systems were demonstrated as well as a range of test equipment for measurements on communication transmission systems.

Standard Telephones and Cables
United Kingdom

Direct Distance Dialing by Hotel Guests—Guests in the Hamburg hotel, Vier Jahreszeiten, can now dial direct, without intervention of the hotel private branch operator, any telephone in a city or country accessible through the automatic public telephone network.

Specifically designed for large hotels, the system will accommodate 320 extensions made up of 220 guest rooms and 100 administration and service stations. Tickets for calls are prepared automatically and give date, called number including toll prefix, number of calling extension, and charge for the call.

Standard Elektrik Lorenz
Germany

***Concorde* Aircraft Research Simulator**—In June 1966 the research simulator manufactured in cooperation with the British company Redifon for the supersonic transport aircraft *Concorde*, was inaugurated in the test laboratories of Sud-Aviation at Toulouse-Blagnac by André Bettencourt, French Minister of Transport.

This simulator, shown in Figure 9, was designed for studying flight characteristics and crew work loads. Experience with it will permit a prototype aircraft to be test-flown with maximum safety. It will also be useful in defining the best flight-deck layout before production starts.

Developed jointly by Sud-Aviation (France) and the British Aircraft Corporation, the maiden flight of the *Concorde* is scheduled for early 1968. Experience with this simulator will influence the development of other flight simulators used for training by the civil airlines that will operate the new aircraft.

Le Matériel Téléphonique
France

Omega Navigation Receivers—The first of a series of microelectronic radio receivers for the Omega navigation system was delivered to the United States Navy. Featuring microelectronic integrated circuits, these sets are scheduled for shipboard sea trials. Other sets are intended for airborne evaluation.

Omega is a very-low-frequency hyperbolic navigation system to provide accurate global coverage.

ITT Federal Laboratories
United States of America

Communication Equipment For Power Station—In Glamorgan, Wales, the Aberthaw B power station of the Central Electricity Board will have an extensive communication system.

A 150-line *PAX 4401* private branch telephone exchange will be connected to an existing exchange to form a single unit. A direct-wire system will allow controllers to communicate with certain locations without passing through the exchange.

A public-address system using 6 amplifiers, each of 150-watt capacity, gives access to 189 loudspeakers. Colored lights for calling personnel to the nearest telephone are operated by dialing a code and identification number from any telephone.

Standard Telephones and Cables
United Kingdom

Blister Packaging—After final inspection small parts may be packed between plastic sheets having blisters specially shaped to fit them. The carbon microphones in Figure 10 are packed between two sheets of polyvinyl chloride. The sheets are 0.02 inch (0.5 millimeter) thick by 19 by 14 inches (480 by 355 millimeters).

Figure 9—Research simulator developed for the supersonic aircraft *Concorde*.

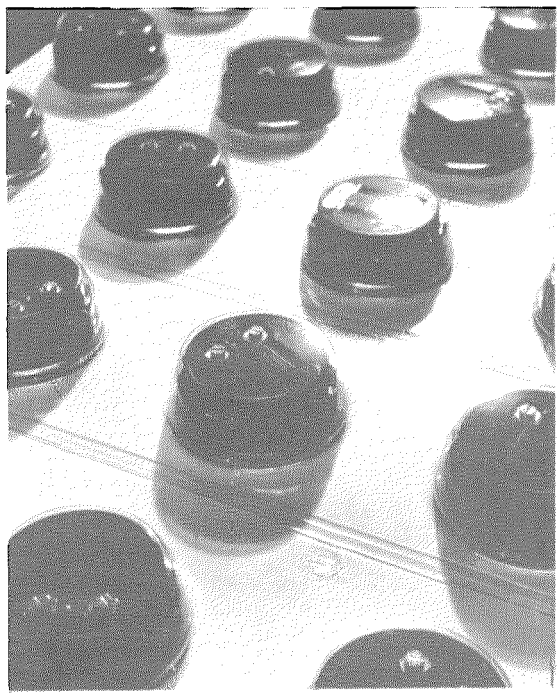

Figure 10—Carbon microphones are packed in clear plastic sheets formed to fit them and sealed by a radio-frequency welder.

The sheets are sealed using a *TP2* welder producing 7 kilowatts at 36, 44, or 51 megahertz obtained from a 440-volt 3-phase supply drawing 20 amperes per phase. The welding equipment will serve two operators on an automatic interlocking work cycle. This system requires only about half the time formerly needed for packing.

Stanelco Industrial Services
United Kingdom

S. S. *Renaissance* Has Pentaconta Equipment—The new 12 000-ton *S. S. Renaissance* of Compagnie Française de Navigation, with accommodations for 416 cabin-class passengers, is the first French ship built solely for cruising. It is equipped with a Pentaconta crossbar telephone system as are other ocean liners such as the *France, Shalom,* and *Sayafjord,* and the oceanographic ship *Jean Charcot.*

The 300-line capacity serves 199 passenger cabins, 54 stations for general passenger services, 2 public telephone booths, the information desk, and the radio room.

Passengers may call each other and all general passenger services. General passenger services may call all stations. Ship's officers may call all stations but cannot be called by passengers. Members of the crew may call all stations but not passengers. When in port, 4 connections to the public telephone network become available through the switching system.

Compagnie Générale de Constructions Téléphoniques
France

Airborne Tacan *AN/ARN-52B*—The design of the new *AN/ARN-52B* Tacan airborne navigation equipment shown in Figure 11 is based on the early *AN/ARN-21*. It includes modules that compute continuously the bearing and distance to the beacon, the display indicators being simple repeaters. Off-track course computers are controlled by mechanical modules without the aid of the bearing and distance indicators. It includes an air-to-air function that allows an aircraft to determine its distance to other aircraft having similar equipment.

It may include either the external cooling nozzles of the conventional *AN/ARN-52* or a special cooling module for automatic operation. Its dimensions are 258 by 393 by 175 millimeters (10.2 by 15.5 by 6.9 inches).

Le Matériel Téléphonique
France

Microelectronic Digital Clock—A prototype model of a microelectronic digital clock has been delivered to the United States Naval Research Laboratory. It is controlled by an external 1-megahertz precision source. Elapsed time is measured by counting and accumulating 1-microsecond intervals in three accumulators, which are automatically synchronized. Error checking and fault location are incorporated.

Monolithic silicon-based integrated circuits are used, requiring only a tenth of the power needed for discrete components. Three separate identical logic chains provide for redundancy.

ITT Federal Laboratories
United States of America

Air-Traffic-Control Ultra-High-Frequency Ground-Station Receiver—The type *E 42-220* receiver for monitoring single channels in the

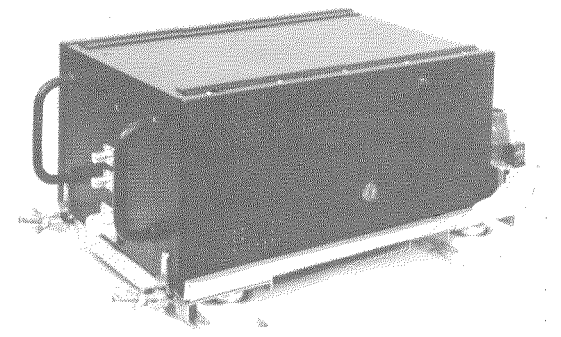

Figure 11—Tacan airborne navigation equipment *AN/ARN-52B.*

air-traffic-control band from 220 to 405 megahertz meets the specifications of the Federal German Administration of Air Navigation Services.

Shelf mounted but readily installed in racks, these transistor receivers are operated from a separate 12-volt power unit capable of supplying up to 8 receivers. A separate meter panel aids in checking the receiver and tuning to a desired channel.

Standard Elektrik Lorenz
Germany

Induction Heating Generator—The *500 HL* radio-frequency generator shown in Figure 12 can be varied to give from a few watts to 500 watts at 1 megahertz. The optimum work-coil inductance is 4 microhenries and requires a water flow of 0.25 imperial gallon (1.14 liters) per minute at 35 pounds per square inch (2.46 kilograms per square centimeter).

Operation from the 200-to-250-volt mains at either 50 or 60 hertz requires 800 watts for full output power. Solid-state diodes are used for rectification. The dimensions are 23 by 22 by 16.5 inches (58 by 55 by 41 centimeters) and the weight is 132 pounds (60 kilograms).

Standard Telephones and Cables
United Kingdom

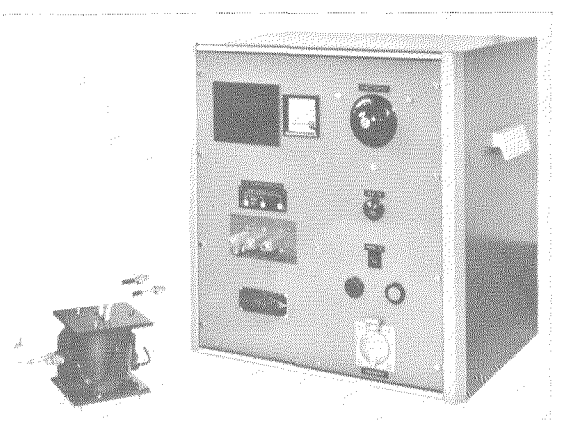

Figure 12—The *500 HL* induction heating generator produces 500 watts at 1 megahertz. A water-cooled work coil is at the left.

Mobile Radiotelephone Equipment—Two new mobile radiotelephone equipments have been developed. The model *LMT 3469 F* transmitter-receiver is for single-channel operation between 68 and 83 megahertz and is intended for taxicab and similar services. The transmitter output is 6 watts.

LMT 3469 G operates on either of two preset channels between 31 and 40 megahertz with a transmitter output of 15 watts. It was developed at the request of an administration having frequencies in this range.

Channel separation for both equipments is 5 kilohertz. Common printed-board subassemblies are easily removed and are interchangeable. Standby power consumption is only 6 watts with 25 and 45 watts, respectively, during transmission. The small size of 220 by 250 by 80 millimeters (8.7 by 9.8 by 3.1 inches) permits simple installation under the instrument board of an automobile. It has been approved by the Telecommunication Administration.

Le Matériel Téléphonique
France

Time—Life International Data Network—Data equipment for transmitting service orders and articles for Time and Life Magazines has been installed in Paris, Bonn, and London with connection to New York via Paris. The public network is used between Paris and London or Bonn. *GH201* data transmission equipment, operating from punched tape at about 150 characters per second, has been supplied by Standard Radio & Telefon (Sweden).

Compagnie Générale de Constructions Téléphoniques
France

Aircraft Beacon 200th Installation—Since 1952, Standard Elektrik Lorenz has manufactured and installed 200 very-high-frequency omnidirectional range (VOR) beacons at airports in Europe, North Africa, America, and Asia. The latest was installed at Djerba in Tunisia. More

than two dozen are in the Federal Republic of Germany.

Standard Elektrik Lorenz
Germany

Ground Surveillance Radar for Artillery Control—Based on the design of a previous battlefield surveillance radar, a new miniaturized system featuring control of artillery fire has been developed. The weight is only about one-tenth that of the previous design using vacuum tubes.[1]

The equipment can be mounted in an armored vehicle, which serves as a command post, or it can be operated in the field as shown in Figure 13. Each unit weighs less than 35 kilograms (75 pounds) for easy handling.

Two prototypes have been delivered to the French Army and have passed field trials. Other nations have expressed interest in the equipment.

Laboratoire Central de Télécommunications
France

[1] Recent Achievements, *Electrical Communication*, volume 40, number 1, page 9; 1965.

Quartz Crystals in Evacuated Glass Envelopes—Three new styles of quartz crystals mounted in evacuated glass envelopes may be seen in Figure 14. They are intended for operation in an ambient up to 150 degrees Celsius. They are available for frequencies between 1.6 and 100 megahertz with close frequency tolerance and improved ageing characteristics.

Standard Telephones and Cables
United Kingdom

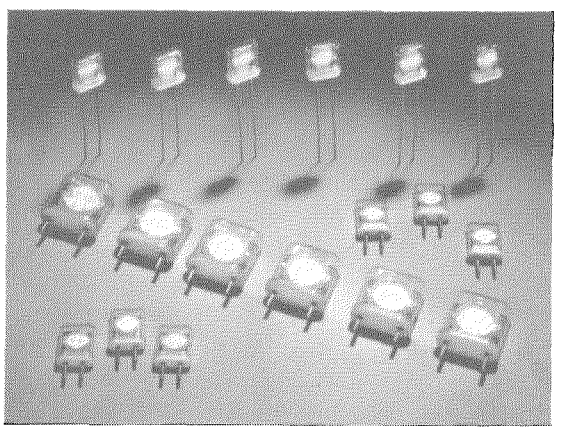

Figure 14—Three new styles of quartz crystal units mounted in evacuated glass envelopes.

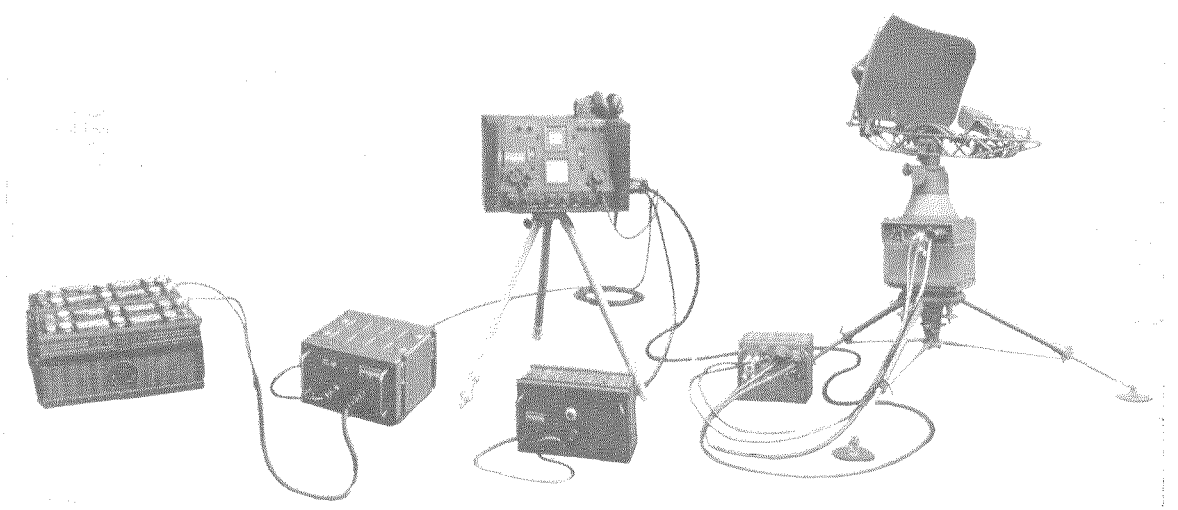

Figure 13—Ground surveillance radar adapted to control of artillery fire. The operator console mounted on a tripod is at the center.

Selbond Television Picture Tube—In a new design of the metal-rim implosion-proof television picture tube, the metal frame embracing the glass viewing screen is made smaller so that it cannot be seen from the front of the set. The screen can extend beyond the front of the cabinet without requiring a plastic mask. A shatter-proof glass protector is not required, thus reducing cost.

As seen in Figure 15, the Selbond design at the top gives the illusion of having a larger screen than the conventional metal-rim tube below.

ITT Standard
Belgium
Standard Elektrik Lorenz
Germany

Precision Potentiometers—A recently developed roller contact reduces the driving torque for a precision potentiometer to 10 gram-centimeters, giving an equivalent noise resistance of 10 ohms. A small unit, *PS18,* with a rating of 3.5 watts is now available in values between 100 ohms and 80 kilohms. The linearity of its 355-degree winding can be held to any precision between 1 percent and 0.2 percent.

The *PS26* has a rating of 5 watts. It is available from 100 ohms to 100 kilohms and a linearity from 1 percent to 0.1 percent.

Standard Telephones and Cables
United Kingdom

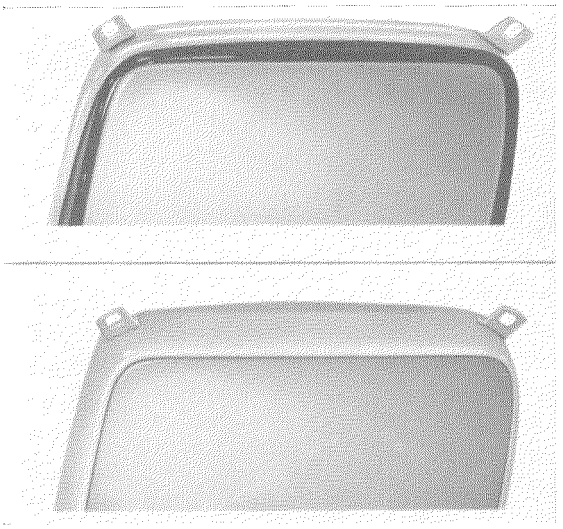

Figure 15—The new type *A59-12W/S* picture tube at top appears to have a wider screen than the conventional metal-rim tube below that it replaces.

Pentaconta Equipment for Petroleum Refining—A modern petroleum refinery operates automatically under control of a computer to which numerous measurements such as liquid level, temperature, and pressure must be reported. A sender associated with each measuring device translates that measurement into a direct current that passes over a 2-wire circuit to the computer and to a receiver for recording. To avoid a very large number of expensive receiver-recorders, advantage is taken of the fact that only a small number of measurements need be recorded simultaneously. This allows a small number of receivers to be connected as required to a much larger number of senders.

As the current from the sender is weak and its analog value is significant, the switching contacts must have high reliability. Pentaconta crossbar telephone equipment with its proved reliability has therefore been installed for switching.

All senders and all receivers are connected to a single control panel. An insulated plug bearing the sender number is inserted in the jack of that sender. To connect this sender to a selected receiver it is necessary only to remove the insulated plug from that jack and insert it in the jack of the selected receiver. The actual connection between sender and receiver is then automatically set up through multiswitches. A checking system automatically signals any abnormal operation. The use of Pentaconta equipment provides not only the required high quality of switching conditions but also the desirable flexibility for expanding to a larger capacity at a later date.

A block diagram of an installation employing 560 senders and 112 receivers is shown in Figure 16.

Compagnie Générale de Constructions Téléphoniques
France

Automatic Letter Sorter—The automatic letter sorter shown in Figure 17 permits 7 operators to sort letters into 100 destination bins. It improves service at the Wiesbaden Post Office in Germany.

Standard Elektrik Lorenz
Germany

Power Supplies for Transistors—A series of stabilized power supply units has been developed in modular construction. The four basic modules shown in Figure 18 can be grouped to fit any particular space requirement.

The output voltage is preset between 0 and a maximum value of 16, 30, or 50 volts. Maximum current is 10 amperes. For an input voltage variation of ±10 percent, the output voltage varies by 0.001 percent in an ambient of 65 degrees Celsius. Operation is from the mains at either 110–125 or 200–250 volts between 45 and 65 hertz.

Standard Telephones and Cables
United Kingdom

Leakage Detector—"Detector 6" is a safety device to operate an alarm or interrupt a system as soon as a set minimum of current flows in the protected circuit. One or more turns of conductor in the circuit to be monitored is threaded through the toroid core of the input transformer, the circular window of which is 100 millimeters (4 inches) in diameter. See Figure 19.

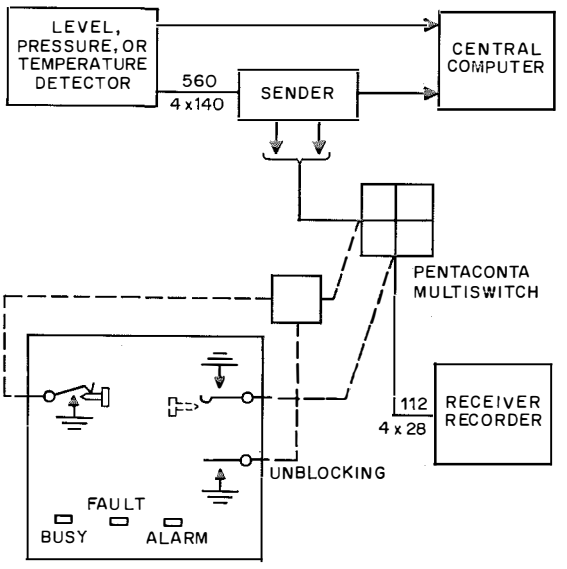

Figure 16—Arrangement of Pentaconta crossbar equipment for connecting 112 receivers to any of 560 senders that measure the level, temperature, and pressure of the product being processed in a petroleum refinery.

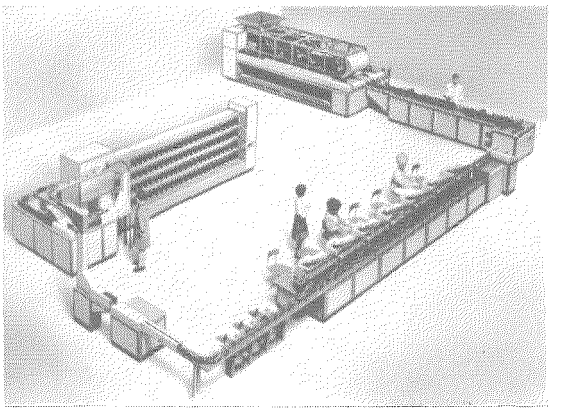

Figure 17—Post-office letter sorter.

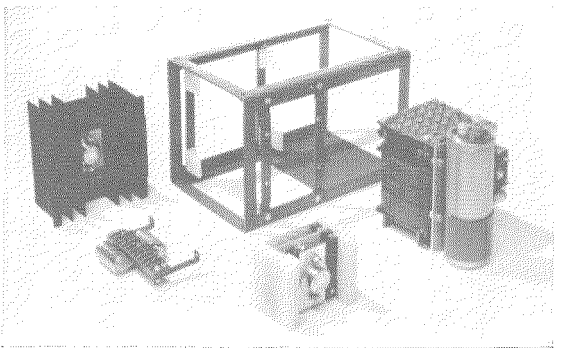

Figure 18—These four modular units for a high-performance power supply for transistors may be grouped in any convenient way to meet space needs.

Transistor amplifiers and a flip-flop circuit pass frequencies up to 50 hertz and reject higher parasitic frequencies. They operate a sensitive relay having make contacts and transfer contacts that handle 5 amperes at 127 alternating volts or 24 direct volts, 3 amperes at 250 alternating volts, or 0.6 ampere at 120 direct volts. The operating threshold of the relay is continuously adjustable from 1 milliampere to 2 amperes in two ranges. The delay between energization and contact closing is 0.5 second. Reset may be either manual or automatic.

Operation is from the 50-hertz mains at either 127 or 220 volts. It is also available for operation at 28 direct volts. The case measures 240 by 135 by 135 millimeters (9.5 by 5.3 by 5.3 inches) and the toroid is 180 by 165 by 165 millimeters (7.1 by 6.5 by 6.5 inches). Weight is approximately 4 kilograms (9 pounds).

Compagnie Générale de Métrologie
France

Impulse Noise Counter—The *74258-A* impulse noise counter shown in Figure 20 can be used to measure the suitability of a voice-frequency circuit for data transmission. Pulses separated by more than 125 milliseconds that exceed a preset limit between 0 and −60 decibels referred to 1 milliwatt are recorded on an internal register. Counting time can be set in fixed steps up to 60 minutes. The register is reset manually and counts to 9999. Additional equipment permits the pulse separation time to be reduced to 100 microseconds.

The equipment meets the requirements of the International Telegraph and Telephone Consultative Committee. It will operate from either internal dry batteries or external direct-current supply. The dimensions are 13 by 10 by 8 inches (33 by 25 by 21 centimeters).

Standard Telephones and Cables
United Kingdom

Peru Orders Crossbar Equipment—Production has started at the East Kilbride factory on a large order for crossbar telephone exchange equipment to be installed in Peru for Compañia Peruana de Telefonos.

Standard Telephones and Cables
United Kingdom

Fiure 19—"Detector 6" for monitoring an electric circuit for leakage currents.

Figure 20—Impulse noise counter.

Transistor-Resistor-Logic Modules—A new series of germanium transistor-resistor-logic modules including NOR and OR gates, buffer amplifiers, pulse shapers, and multivibrators is now available from stock from the Electronic Service Division. They are operable at frequencies up to 5 kilohertz. They are encapsulated with an epoxy resin in polystyrene cases for operation between −10 and +50 degrees Celsius.

Standard Telephones and Cables
United Kingdom

Selective Null Detector—The *96016-A* selective null detector shown in Figure 21 can be used between 25 hertz and 100 kilohertz for bridge balance or as a low-noise preamplifier for oscilloscopes or valve voltmeters.

Sensitivity is 1 microvolt across an input impedance between 25 kilohms and 1 megohm depending on the gain setting. The maximum output is 1 root-mean-square volt across an impedance of 300 ohms in series with 5 picofarads. A switch permits either linear or logarithmic response.

Operation is from 2 internal 6-volt batteries. Dimensions are 9 by 9.8 by 10.9 inches (229 by 248 by 276 millimeters) and the weight is 15 pounds (6.8 kilograms).

Standard Telephones and Cables
United Kingdom

Pentaconta Telephone Exchange for Caravan—It was required that personnel distributed among five vehicles of a caravan be connected with the public telephone network and with each other when stopped during working hours. An automatic crossbar switching system was mounted in a cabinet outside of one of the vans and flexible cables used to extend the system to the other vehicles and the public network.

Compagnie Générale de Constructions Téléphoniques
France

Thyristors Switch Standby Power Supply—It is inconsistent to use moving contacts to switch a load from an alternating-current power main that has failed to a standby inverter if the inverter is equipped with thyristors to avoid contact troubles in generating its alternating-current output. The inverter shown in Figure 22 operates synchronously with the mains and supplies power through a thyristor switch immediately and for the duration of a failure of the mains. Power to the load is uninterrupted and reliability of operation is greatly improved.

Standard Elektrik Lorenz
Germany

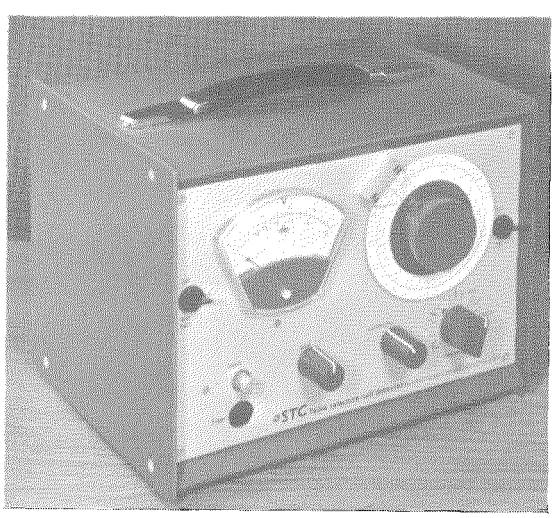

Figure 21—Selective null detector for bridge balancing and similar purposes.

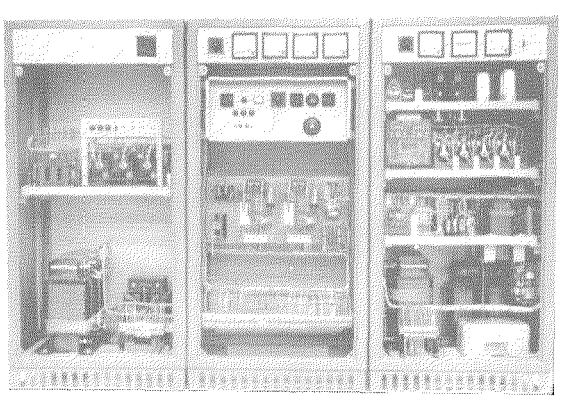

Figure 22—Contactless switching facility.

Other Papers from International Telephone and Telegraph System Authors—April–July 1966

The following list includes papers published in other periodicals and, in some cases, presented at meetings and not yet published. Requests for these unpublished papers should be directed to *Electrical Communication*. Requests for published papers should be made to the indicated publication and not to *Electrical Communication*. The affiliation of the author is given in parentheses.

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Principal ITT System Products

Communication Equipment and Systems

automatic telephone and telegraph central office switching systems...private telephone and telegraph exchanges—PABX and PAX, electromechanical and electronic...carrier systems: telephone, telegraph, power-line, radio multiplex...long-distance dialing and signaling equipment...automatic message accounting and ticketing equipment...switchboards: manual (local, toll), dial-assistance...test boards and desk...telephones: desk, wall, pay-station, special-environment, field sets...automatic answering and recording equipment...microwave radio systems: line-of-sight, over-the-horizon ...teleprinters and facsimile equipment... broadcast transmitters: AM, FM, TV...studio equipment...point-to-point radio communication...mobile communication: air, ground, marine, portable...closed-circuit television: industrial, aircraft, nuclear radiation...slow-scan television...intercommunication, paging, and public-address systems...submarine cable systems...coaxial cable systems

Data Handling and Transmission

data storage, transmission, display...data-link systems...railway and power control and signaling systems...information-processing and document-handling systems...analog-digital converters...alarm and signaling systems... telemetering

Navigation and Radar

electronic navigation...radar: ground and airborne...simulators: aircraft, radar...antisubmarine warfare systems...distance-measuring and bearing systems: Tacan, DMET, Vortac, Loran...Instrument Landing Systems (ILS) ...air-traffic-control systems...direction finders: aircraft, marine...altimeters—flight systems

Space Equipment and Systems

simulators: missile...missile fuzing, launching, guidance, tracking, recording, and control systems...missile-range control and instrumentation...electronic countermeasures...power systems: ground-support, aircraft, spacecraft, missile...ground and environmental test equipment...programmers, automatic...infrared detection and guidance equipment...global and space communication, control, and data systems ...system management: worldwide, local... ground transportable satellite tracking stations.

Commercial/Industrial Equipment and Systems

inverters: static, high-power...power-supply systems...mail-handling systems...pneumatic tube systems...instruments: test, measuring ...oscilloscopes: large-screen, bar-graph...vibration test equipment...pumps: centrifugal, circulating (for domestic and industrial heating)...industrial heating and cooling equipment...automatic controls, valves, instruments, and accessories...nuclear instrumentation

Components and Materials

power rectifiers: selenium, silicon...transistors...diodes: signal, zener, parametric, tunnel ...semiconductor materials: germanium, silicon, gallium arsenide...picture tubes...tubes: receiving, transmitting, rectifier, thyratron, image, storage, microwave, klystron, magnetron, traveling-wave...capacitors: paper, metalized paper, electrolytic, mica, plastic film, tantalum...ferrites...magnetic cores...relays: telephone, industrial, vacuum...switches: telephone (including crossbar), industrial...magnetic counters...magnetic amplifiers and systems...resistors...varistors, thermistors, Silistor devices...quartz crystals...filters: mechanical, quartz, optical...circuits: printed, thin-film, integrated...hermetic seals...photocells, photomultipliers, infrared detectors...antennas...motors: subfractional, fractional, integral...connectors: standard, miniature, microminiature...speakers and turntables.

Cable and Wire Products

multiconductor telephone cable...telephone wire: bridle, distribution, drop...switchboard and terminating cable...telephone cords... submarine cable and repeaters...coaxial cable: air and solid dielectric...waveguides...aircraft cable...power cable...domestic cord sets ...fuses and wiring devices...wire, general-purpose

Consumer Products

television and radio receivers...high-fidelity phonographs and equipment...tape recorders ...microphones and loudspeakers...refrigerators and freezers...air conditioners...hearing aids...home intercommunication equipment... electrical housewares

Microelectronics

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